TWO-LAYER CRYSTAL SQUARE FOR TRANSISTORS ON A SINGLE CHIP

Haissam El-Aawar

Associate Professor, Computer Science/Information Technology Departments
Lebanese International University – LIU
Bekaa-Lebanon
haisso@yahoo.com, haissam.aawar@liu.edu.lb

ABSTRACT

The number of transistors on a chip plays the main role in increasing the speed and performance of a microprocessor; more transistors, more speed. Increasing the number of transistors will be limited due to the design complexity and density of transistors. This article aims to introduce a new approach to increasing the number of transistors on a chip. The basic idea is to construct two-layer crystal square for transistors; this allows to increase the number of transistors two additional times (four times as many) if the number of transistors incorporated in a one layer of crystal square will approximately double every 24 months according to Moore's Law without changing rapidly the design complexity and density in a crystal square and without changing the size of a chip (length and width), in this case the height of a chip must be changed for the two layers.

KEYWORDS

Crystal square, Number of transistors, Feature size, Die size, Design complexity, Density of transistors.

1. INTRODUCTION

Different types of a microprocessor, is also known as a central processing unit (CPU), such as i80x86, Pentium (Intel), PowerPC (IBM), SPARC (Sun), Motorola and many other types perform the same thing in approximately the same way [1].

Moore's Law states that the number of transistors on a chip would double every two years [2, 3]. The designers of CPU are interested to increase the speed and performance of CPU with each new CPU-generation according to the Moore's law by doubling the number of transistors according to the design rule by reducing the size of the transistors, which allows to fit more transistors on a chip without changing rapidly the size of the chip; in general the size of the chip increases slowly over time. Increasing the number of transistors is one of the main factors used to increase the speed and performance of the CPU; more transistors, more clock cycles [4, 5].

2. PHYSICAL LIMITATION OF INCREASING THE NUMBER OF THRANSISTORS

Increasing the number of transistors will be limited due to the following limitation [6, 7, 8, 9]:

2.1 DESIGN RULE, DENSITY AND DESIGN COMPLEXITY [10,11,12,13]

Since the wires and transistors are drawn photographically on the chips, the size of the transistors and the width of the wires are determined by the pixel size of the imaging process. The number of transistors that can be fitted on a given chip size is determined by the size of the transistors. As the feature size on the chip goes down, the number of transistors rises, which means the smaller the transistors, the more transistors can be fitted on the chip. Feature sizes have decreased from 10 micron in 1971 to 0.022 micron in 2012; the semiconductor manufacturing processes have decreased from 10 µm in 1971 to 22 nm in 2012 [4, 13, 14] (see Table 1).

Since the surface area of a transistor determines the transistor count per square millimeter of silicon, the transistors density increases quadratically with a linear decrease in feature size [1]. The increase in transistor performance is more complicated. As the feature sizes shrink, devices shrink quadratically in the horizontal and vertical dimensions. A reduction in operating voltage to maintain correct operation and reliability of the transistor is required in the vertical dimension shrink. This combination of scaling factors leads to a complex interrelationship between the transistor performance and the process feature size.

Due to the shrinking of the pixel size and the increasing of the density, the design complexity increases. If the pixel size shrinks double and the density increases double every two years according to Moore's Law, the physical limitation will definitely appear in few years, which means that it will be very difficult to apply Moore's Law in future. Some studies have shown that physical limitations could be reached by 2018 [6] or 2020-2022 [15, 16, 17, 18].

2.2 NUMBER OF TRANSISTORS AND DIE SIZE [5, 11, 19]

The die size is a size of a chip; the chip size depends on the chip manufacturing processes. As mentioned above, the smaller feature size, the larger number of transistors on a chip, this allows increasing the die size slowly over time. Owing to increasing of the number of transistors the chip size should be increased. The number of transistors of Intel microprocessors has increased from 2300 in 1971 to 3.1 billion in 2012 (1.35 million times during 40 years) and the die size has increased from 12 mm2 in 1971 to 544 mm2 in 2012 (45.34 times during 40 years). The number of transistors of MIPS microprocessors has increased from 110,000 (R2000) in 1986 to 7.15 million (R12000) in 1998 (65 times during 12 years) and the die size has increased from 80 mm2 in 1986 to 229.22 mm2 in 1998 (2.86 times during 12 years). The number of transistors of IBM microprocessors has increased from 1.5 million (Power3) in 1998 to 2.1 billion (Power7+) in 2012 (1400 times during 14 years) and the die size has increased from 270 mm2 in 1998 to 567 mm2 in 2012 (2.1 times during 14 years) (see Table 1).

2.3 PIXEL SIZE AND POWER CONSUMPTION [1,20]

The transistor's switching speed is determined by the pixel size, the smaller transistors switch faster, so they require less power to be switched. Small pixel size allows the battery life of portable devices to be saved for a long time. The energy consumption required for switching transistors is known as dynamic power consumption, which can be increased due to charging and discharging the capacitive output load. Increasing the amount of power requires more hot generation, which can cause an interference of transistors with each other.

Table 1. Evolution of Microprocessors: 1991 to 2012

Manufacturer	Processor	Date of introduction	Number of transistors	Process	Area [mm²]
Intel	Intel4004	1971	2,300	10 µm	12
	Intel8008	1972	3,500	10 µm	14
	Intel8080	1974	4,400	6 µm	20
	Intel8085	1976	6,500	3 µm	20
	Intel8086	1978	29,000	3 µm	33
	Intel80286	1982	134,000	1.5 µm	44
	Intel80386	1985	275,000	1.5 µm	104
	Intel80486	1989	1,180,235	1 µm	173
	Pentium	1993	3,100,000	0.8 µm	294
	Pentium Pro	1995	5,500,000	0.5 µm	307
	Pentium II	1997	7,500,000	0.35 µm	195
	Pentium III	1999	9,500,000	0.25 µm	128
	Pentium 4	2000	42,00,000	180 nm	217
	Itanium 2 McKinely	2002	220,000,000	180 nm	421
	Core 2 Duo	2006	291,000,000	65 nm	143
	Core i7 (Quad)	2008	731,000,000	45 nm	263
	Six-Core Core i7	2010	1,170,000,000	32 nm	240
	Six-Core Core i7/8-Core Xeon E5	2011	2,270,000,000	32 nm	434
	8-Core Itanium Poulson	2012	3.100,000,000	32 nm	544
MIPS	R2000	1986	110,000	2.0 µm	80
	R3000	1988	150,000	1.2 µm	56
	R4000	1991	1,200,000	0.8 µm	213
	R10000	1994	2,600,000	0.5 µm	299
	R10000	1996	6,800,000	0.35 µm	299
	R12000	1998	7,1500,000	0.25 µm	229
IBM	POWER3	1998	15,000,000	0.35 µm	270
	POWER4	2001	174,000,000	180 nm	412
	POWER4+	2002	184,000,000	130 nm	267
	POWER5	2004	276,000,000	130 nm	389
	POWER5+	2005	276,000,000	90 nm	243
	POWER6+	2009	790,000,000	65 nm	341
	POWER7	2010	1.200,000,000	45 nm	567
	POWER7+	2012	2.100,000,000	32 nm	567

3. TWO-LAYER CRYSTAL SQUARE

This article suggests as a solution for avoiding the physical limitations mentioned above and for applying Moore's Law more years a new approach of constructing a crystal square contained transistors on a chip. This approach is called two-layer crystal square of transistors.

Assume a microprocessor (let's say X) has the following specifications: date of introduction – 2015, one-layer crystal square of transistors, transistor count (number of transistors) – 3 billion, pixel size (feature size) – 0.038 micron, die size (area) – 600 mm2 (see Figure 1).
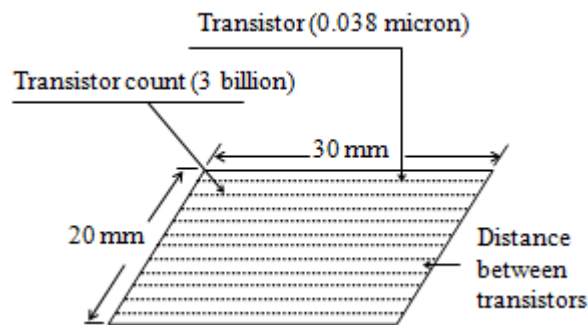

Figure 1. Crystal Square of Transistors

A crystal square of transistors can be constructed using two layers that are equal in size and transistor count, this allows to increase the number of transistors twice (Moore's Law) without touching the feature size and die size (see Figure 2).
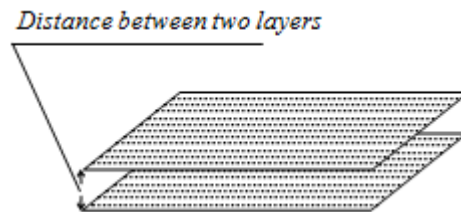

Figure 2. Two-Layer Crystal Square of Transistors

The two-layer crystal square of transistors shown in Figure 2 contains double transistor count without changing feature size and die size. Double number of transistors allows increasing a microprocessor's speed approximately twice. In this case the voltage of transistors must be decreased in order to reduce the dynamic power and energy.

Assume the second generation of the microprocessor (X1) has the following specifications: date of introduction – 2017, Two-layer crystal square, and each layer with the following characteristics: number of transistors – 3 billion (6 billion both), pixel size – 0.038 micron, die size – 600 mm2 (see Figure 3).

Transistor (0.038 micron)

Transistor count (3 billion)

Distance between two layers
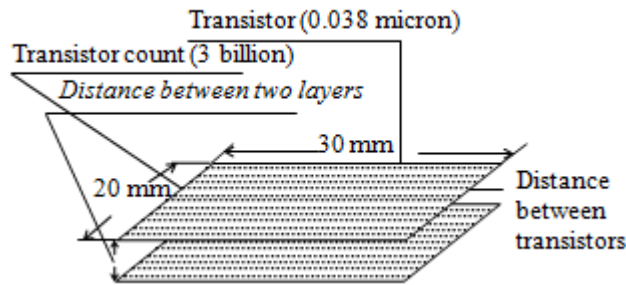
30 mm

20 mm

Distance between transistors

Figure 3. Second Generation

Applying this approach would double transistor count and speed of the microprocessors every two years with slowly increasing the density and area, and decreasing feature size and voltage, so the physical limitations will be reduced and Moore's Law will be continued for many years (may be till 2037 or more).

Assume the third generation of the microprocessor (X2) has the following specifications: date of introduction – 2019, Two-layer crystal square, and each layer with the following characteristics: transistor count – 6 billion (12 billion both), pixel size – 0.035 micron, die size – 688 mm2 (see Figure 4).

Transistor (0.035 micron)

Transistor count (6 billion)

Distance between two layers
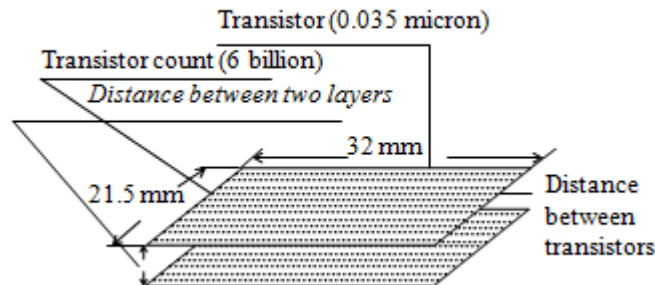
32 mm

21.5 mm

Distance between transistors

Figure 4. Third Generation

The third generation doubles the transistor count with small decreasing of the feature size (from 0.038 micron to 0.035 micron) and small increasing of the area (from 600 mm2 to 688 mm2), of course, with more density, which allows to fit more transistors in small area.

All the assuming characteristics of the microprocessors (X, X1, X2) and others (XN-1 and XN) are shown in Table 2. This table shows some of the assuming microprocessors from 2015 till the year 2037. The number of transistors will have doubled every two years. The feature size will have increased 3 nm (from 38 to 35) every two years (from the year 2019 – after applying a two-layer crystal technology in the year 2017), which means that the feature size would be reached 0.8 nm by the year 2037, which increases the design complexity and causes reaching the physical limitation. The area will also have increased about 12-15% every two years (from the year 2019); the small increasing of area can be applied if and only if the density of transistors increases with each generation. The increasing of the density would also be reached the physical limitation by the year 2037, as more density needs more power, which requires more hot generation.

Table 2. Assuming Evolution of Microprocessors: 2015 to 2037

Processor	Date of introduction	Number of transistors (billion)	Feature size (nm)	Area [mm^2]
X	2015	3	38	600
X1 (Two-layer crystal)	2017	6	38	600 (each layer)
X2 (Two-layer crystal)	2019	12	35	688 (each layer)
X3 (Two-layer crystal)	2021	24	32	770 (each layer)
X4 (Two-layer crystal)	2023	48	29	882 (each layer)
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XN-1 (Two-layer crystal)	2035	3072	11	---
XN (Two-layer crystal)	2037	6144	0.8	---

As shown in the table below, several measures of microprocessors technology, such as transistor count, is improving at exponential rate based on Moore's Law (see Figure 5).
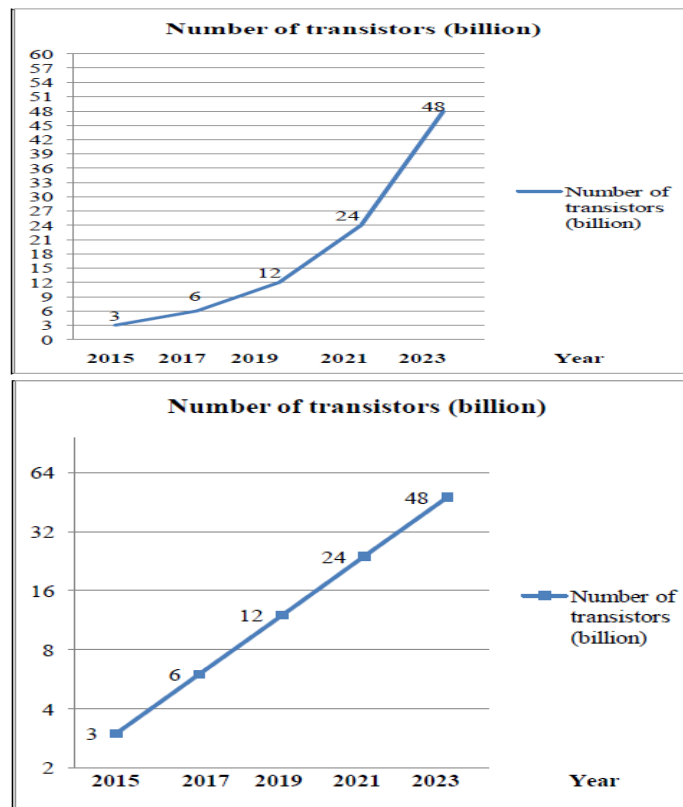

Figure 5. Number of transistors related to Moore's Law

4. CONCLUSION

The problem of applying Moore's law in microprocessor technology as much as possible is still topical research field although it has been studied by the research community for many decades. The main objective of this article is to find as much as possible a complete and logical solution for avoiding physical limitation in manufacturing of microprocessors technology and applying Moore's Law for a long time.

As mentioned above, some studies have shown that physical limitations could be reached by 2018 or 2022. Applying the new approach in microprocessor technology will delay the physical limitation for few more years, because it doubles the transistor count every two years based on Moore's Law, which approximately double the microprocessor's speed, with small decreasing of the feature size and small increasing of the area.

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AUTHOR

Haissam El-Aawar is an Associate Professor in the Department of Computer Science and Information Technology at the Lebanese International University where he has been a faculty member since 2009. Haissam completed his Ph.D. and M.Sc. degrees at the State University "Lviv Polytechnic" in Ukraine. His research interests lie in the area of Artificial Intelligence, theory of complexity, microprocessors evaluation, CISC- and RISC-architectures, robotics control, mobility control and wireless communication.