PERFORMANCE COMPARISON OF 4T, 3T AND 3T1D DRAM CELL DESIGN ON 32 NM TECHNOLOGY

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ABSTRACT

In this paper average power consumption of dram cell designs have been analyzed for the nano-meter scale memories. Many modern processors use dram for on chip data and program memory. The major contributor of power in dram is the off state leakage current. Improving the power efficiency of a dram cell is critical for the improvement in average power consumption of the overall system. 3T dram cell, 4T dram and 3T1D DRAM cells are designed with the schematic design technique and their average power consumption are compared using TANNER EDA tool .average power consumption, write access time, read access time and retention time of 4T, 3T dram and 3T1D DRAM cell are simulated and compared on 32 nm technology.

KEYWORDS

Low Power, DRAM, 3TDRAM, 4TDRAM, 3T1D DRAM

1. INTRODUCTION

Memories play an essential role in design of any electronics design where storage of data is required. Memories are used to store data and retrieve data when required. Read Only Memory (ROM) and Random Access Memory (RAM) are two types of memories used in modern day architectures. Random Access Memory is of two types Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM). SRAM is static in nature and faster as compared to DRAM.SRAM is expensive and consume less power. SRAM have more transistors per bit of memory. They are mostly used as cache memories. DRAMS on the other hand are dynamic in nature and slower as compared to SRAM. DRAM are expensive and consume more power, they require less transistor per bit of memory. They are mostly used as main memories. DRAM is widely used for main memories in personal and mainframe computers and engineering workstation. DRAM memory cell is used for read and write operation for single bit storage for circuits. A single DRAM cell is capable of storing 1 bit data in the capacitor in the form of charge. Charge of the capacitor decreases with time .Hence refresh signals are used to refresh the data in the capacitor. When a read signal reads the data it refreshes it as well. Many different cell designs exist for modern day DRAM cell. These designs are differentiated by the no. of transistors used in their designing. As the no. of transistors increase, power dissipation also increases. DRAM is one of the most common and cost efficient random access memory used as main memory for workstations. The charge stored in memory cell is time dependent. For high density memories DRAM cell with low power consumption and less area are preferred.

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Many different cell designs exist for modern day DRAM cell. These designs are differentiated by the no. of transistors used in their designing. As the no. of transistors increase, power dissipation also increases. DRAM is most common and cost efficient random access memory used as main memory for workstations. The charge stored in memory cell is time dependent. First DRAM was proposed in 1971, having 1 kb capacity. This capacity has increased from 1kb to 1-10 GB level today.

2. LITREATURE SURVEY

2.1. Static random access memory (SRAM)

Structure**:** SRAM provide static random access memory implementation. Here 6 transistors are used to store bits of data. SRAM 6T form L1 data cache in microprocessor as they have short access time, they are able to retain data for 10's of microsecond. Current level of device miniaturizations makes it very difficult to model 6T SRAM memories with required level of reliability 6T SRAM also suffers from instability which results in performance reduction, which helps in gaining technology scaling. [3]. Process variation directly attaches the weakness of 6T SRAM producing transistors that deviate from their sizes , thereby causing device mismatches .Process variation directly attaches the weakness of 6T SRAM producing transistors that deviate from their sizes ,thereby causing device limits 6T performance scalability by causing variation in operating speed of individual cells and memory lines. [4]

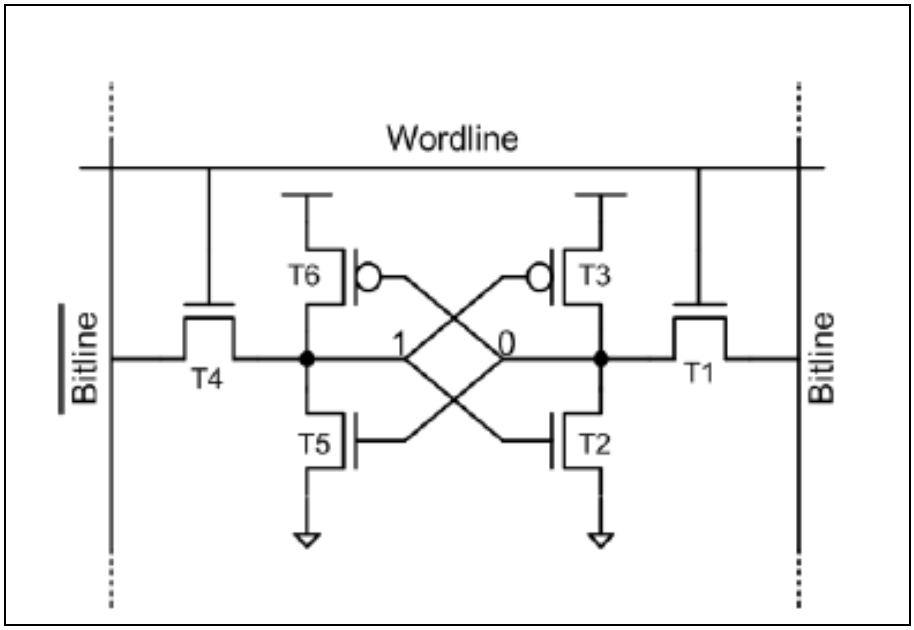

Fig.1 Schematic 6T SRAM

Process variation affects speed of 6T SRAM. Figure shows schematic of standard 6T cell. To perform read operation pre-charging of both bit-lines, strobing word line and seeing which bit-line discharges. If inverted then '1' is read if regular then '0'.Variation in gate length and threshold voltages of these transistors changes current driving capabilities. Process variation also attacks the stability of a 6T SRAM cell. For example, transistor T2 is designed to be very strong, transistor T1, moderately strong, and transistor T3, weak.

In reads, this allows T2 to quickly discharge the necessary bit-line while ensuring the intermediate node between T2 and T3 does not rise enough to store a 1 when it is supposed to store a 0. Any variation within the cell changes the strength of each transistor, and may lead to a weaker T2 that does not discharge the bit-line quickly enough. Such variation allows the value at the intermediate node to rise completely and flip the bit stored in the circuit, causing a pseudo-destructive read. The same analysis holds for transistors T4, T5, and T6. Variation also causes instability in writes. [5]

2.2. 1T1C DRAM Cell:

The information is stored as different charge levels at a capacitor in conventional 1T/1C DRAM. The advantage of using DRAM is that it is structural simple: only one transistor and capacitor are required for storing one bit, compared to six transistors required in SRAM. This allows DRAM to have a very high density. The DRAM industry has advanced over a period of time in packing more and more memory bits per unit area on a silicon die. But, the scaling for the conventional 1Transistor/1Capacitor (1T/1C) DRAM is becoming increasingly difficult, in particular due to a capacitor has become harder to scale, as device geometries shrink. Apart from the problems associated with the scaling of the capacitor, scaling also introduces yet another major problem for the DRAM manufacturers which is the leakage current.

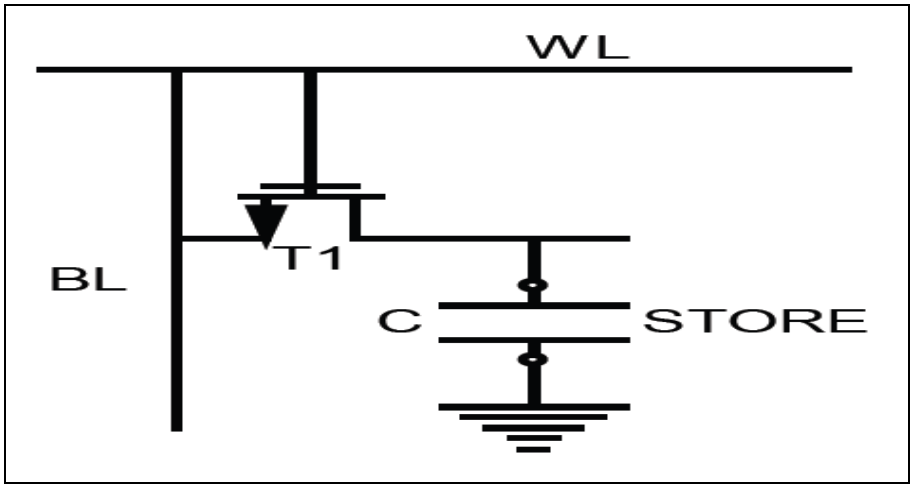

Fig. 2 Schematic 1T1C DRAM cell

2.3. 4T DRAM Cell:

The cell structure shown in fig. 3 is a 4T DRAM cell structure. This DRAM cell design consists of four transistors. One transistor is used as a write transistor, the other as a read transistor. Data in DRAM is stored in the form of charge at the capacitance attached with the transistor structure. There is no current path to the storage node for restoring the data; hence data is lost due to leakage with the period of time. Read operation for the 4T DRAM cell is non-destructive, as the voltage at the storage node is maintained.

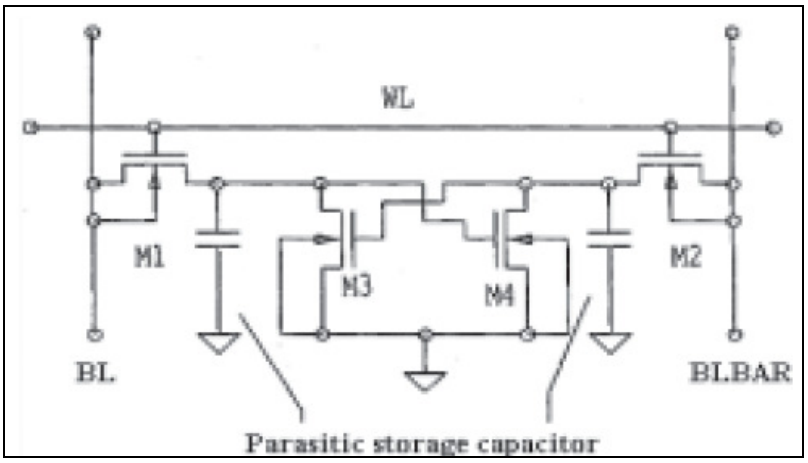

Fig. 3 4T DRAM CELL

2.4. 3T DRAM Cell:

The simplest DRAM cell is the 3T scheme. A 3T DRAM cell has a higher density than a SRAM cell; moreover in a 3T DRAM, there is no constraint on device ratios and the read operation is nondestructive. In this cell, the storage capacitance is the gate capacitance of the readout device, so making this scheme attractive for embedded memory applications; however, a 3T DRAM shows still limited performance and low retention time to severely limit its use in advanced integrated circuits.3T DRAM utilizes gate of the transistor and a capacitance to store the data value. When data is to be written, write signal is enabled and the data from the bit line is fed into the cell. When data is to be read from the cell, read line is enabled and data is read through the bit line. 3T DRAM cell occupies less area compared to the 4T DRAM cell (fig. 4).

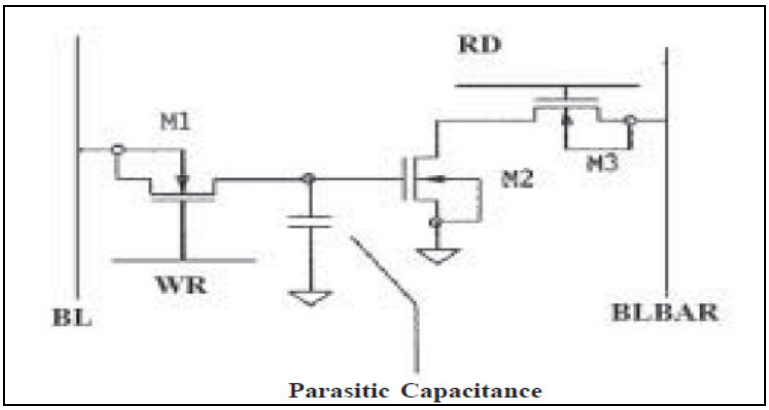

Fig. 4 3T DRAM CELL

2.5. 3T1D DRAM Cell:

This is a DRAM structure derived from 3T cell, like all DRAM it uses few transistor compared to static random access memory (SRAM). The 3T1D has an advantage over SRAM, is its resistance to process variation, this feature helps it to be used at low feature sizes. Another advantage of 3T1D DRAM is that it does not slow down as its size is scaled down.3T1D DRAM uses the gated

diode instead of capacitor to store the data value. The absence of capacitor provides significance reduction in power consumption as compared to previous DRAM cell design.

In order to write the cell at the BL write line level, it is only required to activate T1 through the WL write line. Hence, the S node stores either a 0 or a VDD−Vth voltage depending on the logic value. This voltage results in the accumulation of charge at the gate of devices D1 and T2. [2]

The 3T1D cell in fig. 5 shows the scheme of the basic cell. The basis of the storage system is the charge placed in node S, written from BL write line when T1 is activated. Consequently, it has a DRAM cell nature, but it allows a non-destructive read process (a clear advantage over 1T1C memories) and high performance read and writes operation, comparable to 6T.With T1 and T3 transistors as accessing devices, the whole cell is composed by four transistors of similar size to the corresponding of 6T.

This implies a more compact cell structure. In order to write the cell at the BL write line level it is only required to activate T1 through the WL write line. Hence, the S node stores either a 0 or a VDD-Vth voltage depending on the logic value. This voltage results in the accumulation of charge at the gate of devices D1 and T2.A key aspect of the 3T1D memory cell is that the capacitance of the gated diode (D1) when Vgs is above Vth is significantly higher with respect to lower voltages, because there is a substantial amount of charge stored in the inversion layer.

In order to read the cell, the read bit line BL read has to be previously pre-charged at VDD level. Then T3 is activated from WL read line. If a high (1) level is stored in S, transistor T2 turns on and discharges the bit line. If a low (0) level is stored in S, transistor T2 does not reach enough conduction level. The objective of the gated diode D1 is to improve Read Access Time. When a high (1) level is stored in S, D1 connected to WL read line causes a boosting effect of the voltage level in node S. The voltage level reached at node S is close to Vdd voltage causing a fast discharge of the parasitic capacitance in BL read. If allow (0) level is stored, transistor T2 keeps turned off. [9]

Variability introduces a wide range of effects, especially on the performance of integrated circuits. Some of them appear during the manufacturing process, others during the working life, and all of them have as a consequence a decrease in the circuit reliability. In the case of 3T1D memory cell, all the possible variations can be lumped into a timing degradation. In this sense 3T1D tolerates higher levels of variability than 6T cell, which incurs into timing degradation as well as instability. [1]

Manufacturing process introduces variations in devices characteristic parameters, such as threshold voltage and physical dimensions (length and width) of transistors. These variations can be classified depending on their statistics as systematic (inter die and intra-die systematic) or random (intra-die random). To simulate these effects in a single cell we use a Gaussian distribution. Systematic variability is assumed to be the same for all the transistors in a single cell, while random variability is calculated independently for each transistor. Another key point is that this kind of variation remains static during the whole life of a circuit because it depends only on the manufacturing process. [2]

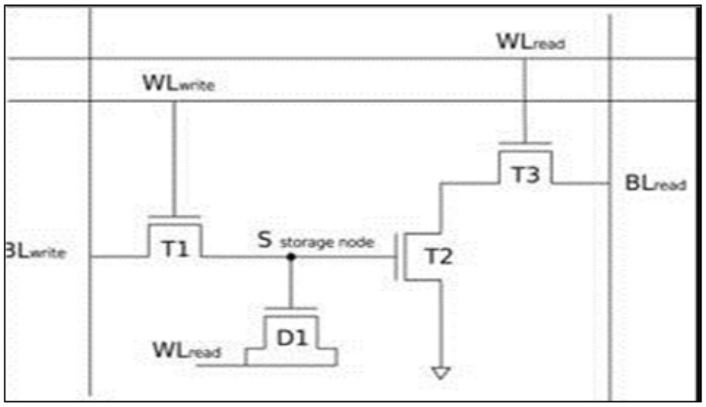

Fig. 5 3T1D DRAM CELL

3. SCHEMATICS OF CELLS

All simulation carried out on TANNER EDA 14.0 with model file of 32nm high performance taken from PTM. Tool used for circuit design is SEDIT and for simulation is TSPICE.

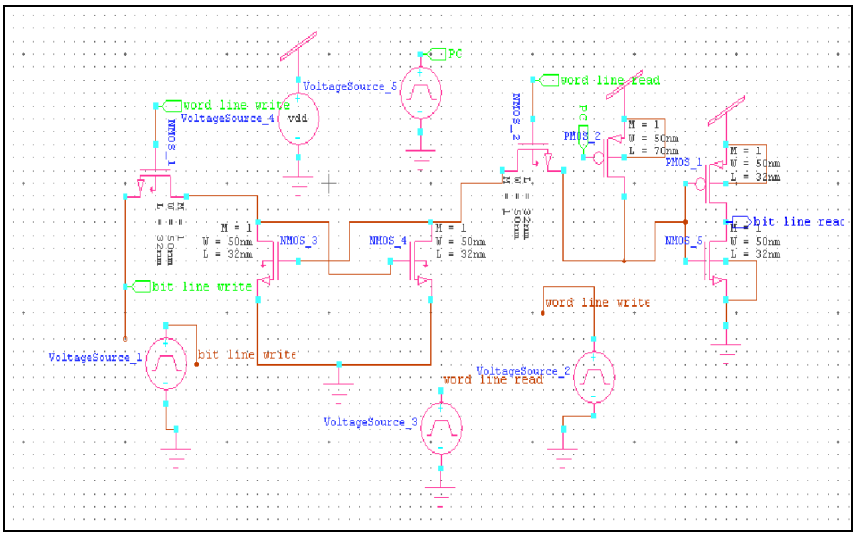

Fig. 6 Schematic of 4T DRAM

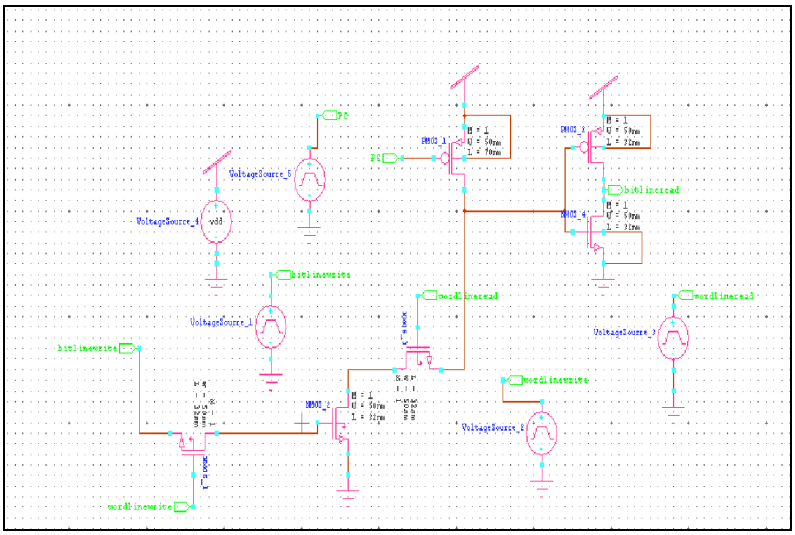

Fig.7 Schematic of 3T DRAM

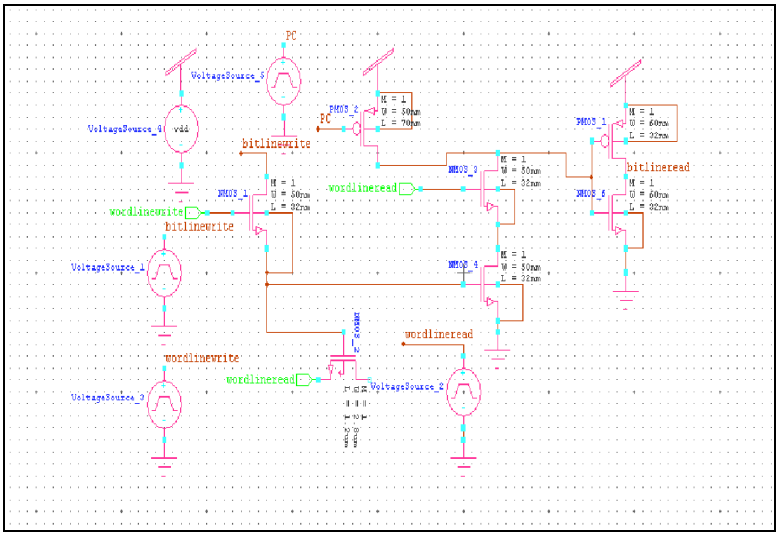

Fig.8 Schematic of 3T1D DRAM

4. SIMULATION RESULTS

Simulation for all five cells 4T, 3T,3T1D ,Gain 3T,Power modified 3T1D design are carried out from 0-10 ns. During this interval all the four process write ‘0’, write ‘1’, read ‘0’ and read ‘1’,are executed. Average power consumption is calculated for the full 0-10ns duration consisting of all four operations.

Table1. Operation of waveforms

Operation	Time Period
WRITE ‘1’	2-3ns
READ ‘1’	4-5ns
WRITE ‘0’	6-7ns
READ ‘0’	8-9ns

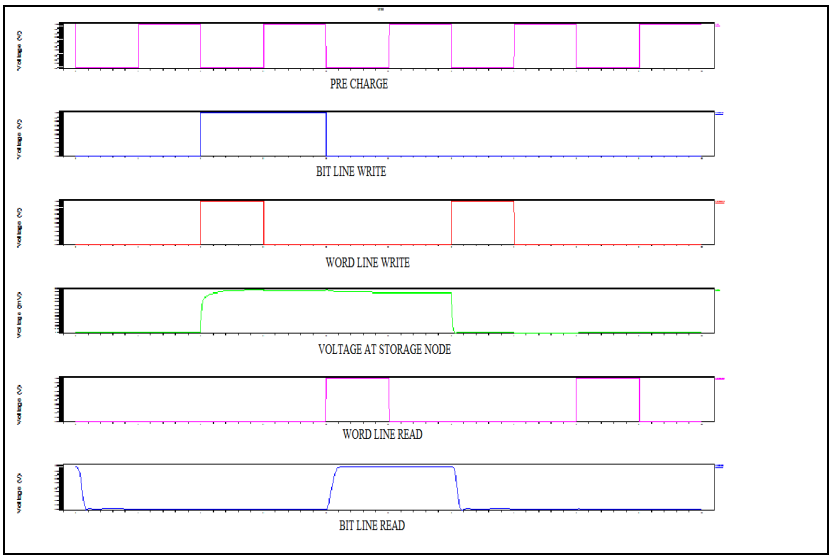

Fig.9 Read Write operation of 4T DRAM Cell

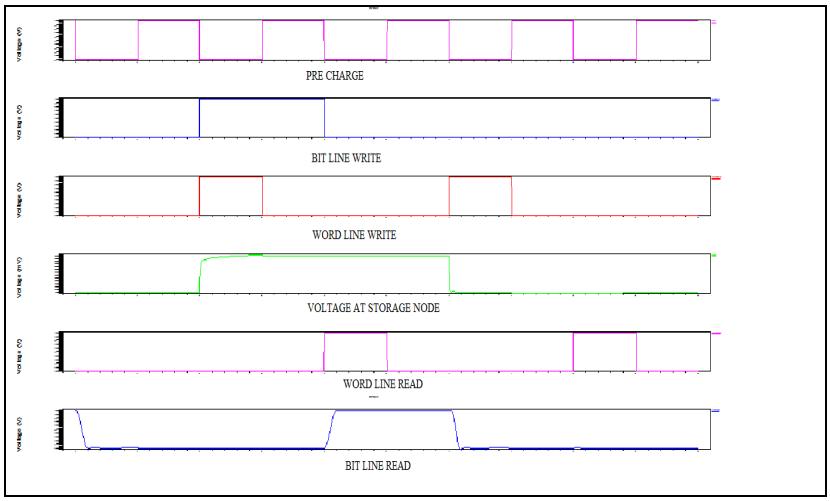

Fig.10 Read Write operation of 3T DRAM Cell

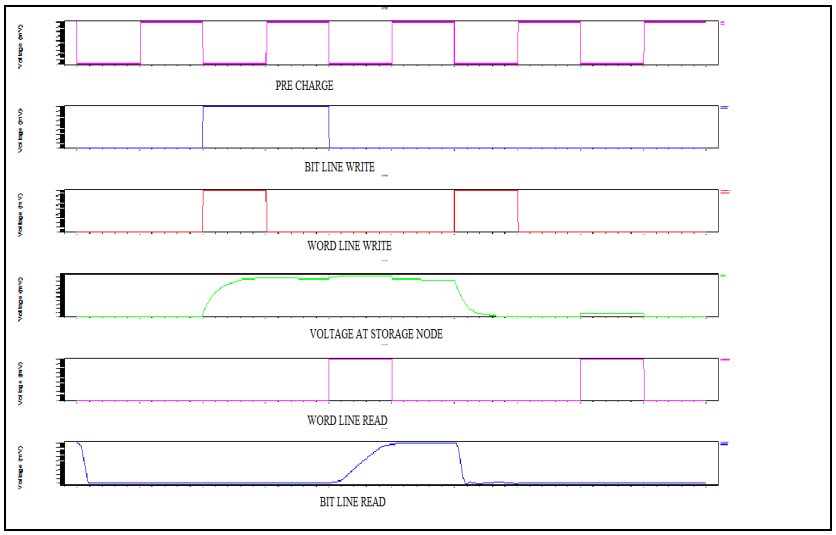

Fig.11 Read Write operation of 3T1D DRAM Cell

5. PERFORMANCE ANALYSIS

Average power consumption foe 4T, 3T, 3T1D, gain 3T and Power modified 3T1D is carried out. The average power consumption value is calculated with varying temperature form 20˚C to 100˚C. It is essential to perform power v/s temperature as it gives an idea about the average power consumption of the cell design when it is subjected to high temperature.

Table2. Average Power Consumption V/S Supply Voltage

SUPPLY VOLTAGE (volt)	AVERAGE POWER CONSUMPTION FOR 4T(u watt)	AVERAGE POWER CONSUMPTION FOR 3T(u watt)	AVERAGE POWER CONSUMPTION FOR 3T1D(u watt)
0.7	0.1656537	0.2507752	0.1299199
0.8	0.2625748	0.6496773	0.3846698
0.9	0.6618851	1.167894	1.255590
1	1.739659	1.662307	1.566112
1.1	2.384711	2.262632	2.170092

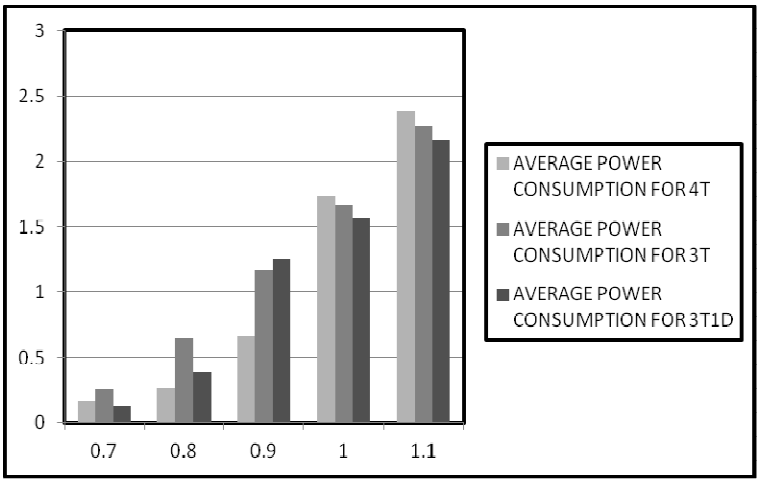

Fig. 12 Bar chart comparing power consumption of dram cell with supply voltage

Table3. Write Access Time V/S Supply Voltage

SUPPLY VOLTAGE (volt)	WRITE ACCESS TIME FOR 4T (p sec)	WRITE ACCESS TIME FOR 3T (p sec)	WRITE ACCESS TIME FOR 3T1D (p sec)
0.7	25.43	16.6	230.09
0.8	27.28	17.66	281.40
0.9	26.96	17.56	291.17
1	35.73	19.53	299.35
1.1	37.45	20.89	385.45

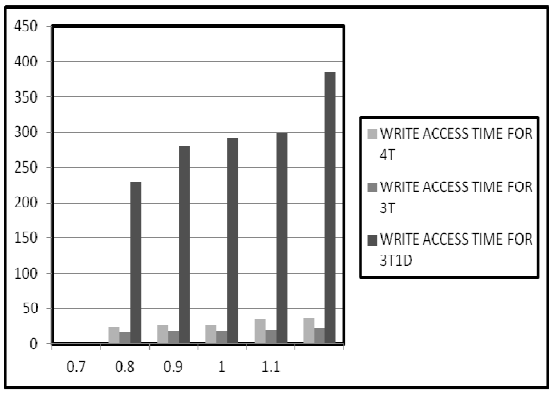

Fig. 13 Bar chart comparing write access time of DRAM cell with supply voltage

Table4. Read Access Time V/S Supply Voltage

SUPPLY VOLTAGE (volt)	READ ACCESS TIME FOR 4T (p sec)	READ ACCESS TIME FOR 3T (p sec)	READ ACCESS TIME FOR 3T1D (p sec)
0.7	----	----	----
0.8	----	----	----
0.9	----	181.86	506.43
1	100.87	87.72	103.40
1.1	71.19	70.7	68.65

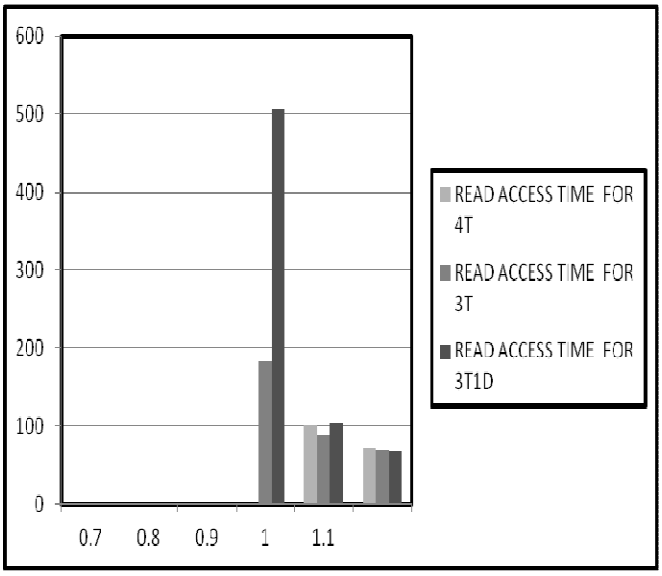

Fig. 14 Bar chart comparing read access time of DRAM cell with supply voltage

Table5. Retention Time V/S Supply Voltage

SUPPLY VOLTAGE (volt)	RETENTION TIME FOR 4T (u sec)	RETENTION TIME FOR 3T (u sec)	RETENTION TIME FOR 3T1D (u sec)
0.7	4.54378	5.31742	66.44272
0.8	4.02719	4.50587	59.30578
0.9	3.09407	3.44944	52.44869
1	2.61674	3.74946	45.55423
1.1	2.45621	3.49827	40.07223

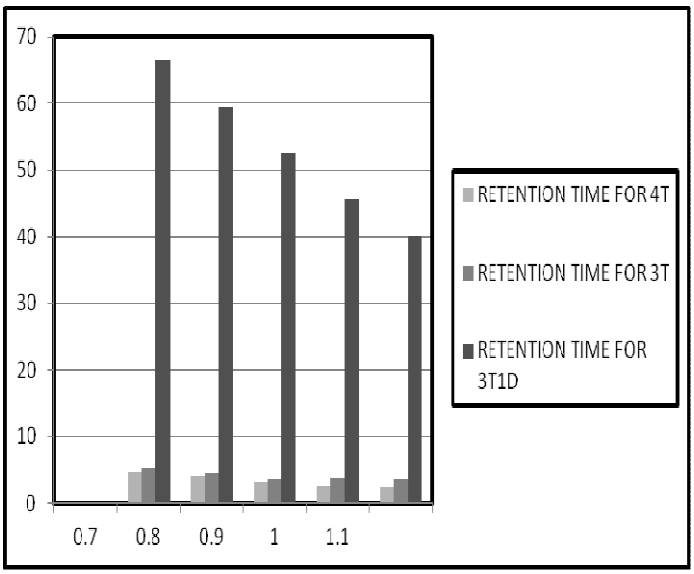

Fig. 15 Bar chart comparing retention time of dram cell with supply voltage

6. CONCLUSION

The study of 4T DRAM cell, 3T DRAM cell and 3T1D DRAM cell for average power consumption, write access time, read access time and retention time has been carried out. These parameters are studied in accordance with variation of supply voltage FROM 0.7, 0.8, 0.9, 1.0, 1.1V.

Analysis of Average Power Consumption shows that 3T1D DRAM cell has the least average power consumption compared to 4T DRAM and 3T DRAM cell. Average Power Consumption tends to increase as the supply voltage increases.

Analysis of Write Access Time shows that 3T DRAM cell has the least write access time compared to 4T DRAM and 3T1D DRAM cell. Write Access Time of 3T1D DRAM is significantly more than that of 3T and 4T DRAM cell. Write Access Time tends to increase as the supply voltage increases.

Analysis of Read Access Time shows that 3T DRAM cell has the least read access time compared to 4T DRAM and 3T1D DRAM cell. Read Access Time of 3T1D DRAM is significantly more than that of 3T and 4T DRAM cell. Read Access Time tends to decrease as the supply voltage increases.

The most significant parameter for DRAM cell is retention time. 4T DRAM cell has the least retention time among the three cells. The retention time for 3T1D DRAM cell is significantly more than that of 4T and 3T DRAM cell. Retention time tends to decrease as the supply voltage increases.

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