LOW POWER VLSI COMPRESSORS FOR BIOMEDICAL APPLICATIONS

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ABSTRACT

We present a new design for a 1-bit full adder featuring hybrid-CMOS design style. Our approach achieves low-energy operations in 90nm technology. Hybrid-CMOS design style makes use of various CMOS logic style circuits to build new full adders with desired specifications. The new SERF- full adder (FA) circuit optimized for ultra low power operation is based on modified XOR gates with clock gating to minimize the power consumption. And also generates full-swing outputs simultaneously. The new full-adder circuit successfully operates at low voltages with excellent signal integrity. The new adder displayed better power and delay metrics as compared to the standard full adders. To evaluate the performance of the new full adder in a real circuit, we realized 4-2,5-2,5-3,7-2,11-2,15-4,31-5 compressors which are basically used in multiplier modules of DSP filters. Simulated results using 90nm standarad CMOS technology are provided. The simulation results show a 5% - 20% reduction in power and delay for frequency 50MHz and supply voltages range of 1.1 v.

KEYWORDS

SERF Full adder, ultra low power

1. INTRODUCTION

The demand for mobile electronic devices of low-power and high-speed is driving designers to design for smaller silicon area, high speed, longer battery life and more reliability. Power dissipation is the limiting factor for hand held devices. as energy-efficiency is one of the most required features for high-performance and/or portable applications. The power-delay product (PDP) metric relates the amount of energy spent during the realization of a determined task, and stands as the more fair performance metric. For high performance design. microprocessors and digital signal processors rely on the efficient implementation of generic arithmetic logic units and floating point units to execute dedicated algorithms such as convolution and filtering [4].In most of these applications, multipliers have been the critical component and adder cells are in the

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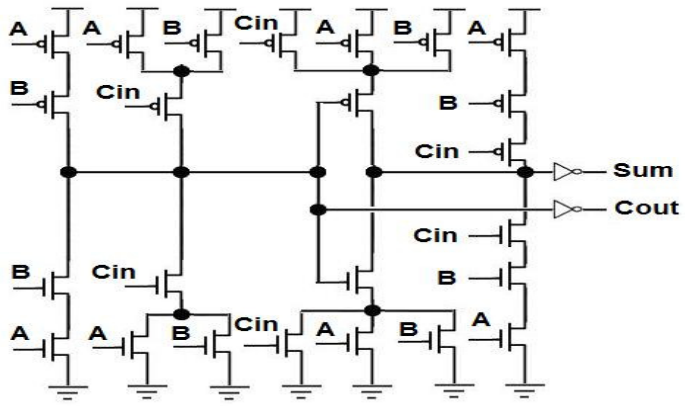
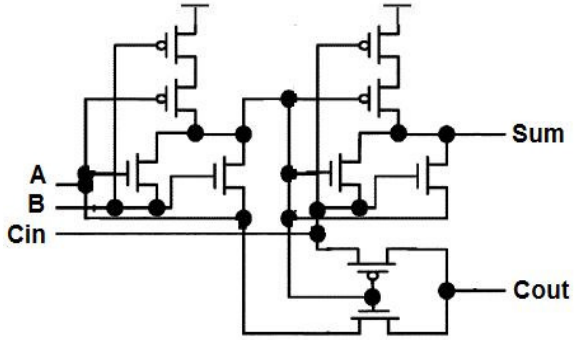
critical paths of these complex arithmetic modules. Therefore design of ultra low power circuits becomes critical for portable applications. Addition is a fundamental arithmetic used in application-specific digital signal processing (DSP) architectures and is the core of many arithmetic operations such as addition/subtraction, multiltiplication, division and address generation. Thus, the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems. At the circuit level, an optimized design is desired to avoid any degradation in the output voltage, consume less power, have less delay in critical path, and be reliable even at low supply voltage as we scale towards deep submicrometer. However, for ultra low power applications like implants and wireless sensor nodes, the most important design goal is to optimize for low power consumption. Digital hearing aids frequently employ the concept of filter banks whose complexity of computation requires more number of multiplications of higher power consumption. Therefore the construction of filter bank in Digital hearing aid with minimum number of multiplications is a desired design option. [11] Booth Wallace multiplier is used for implementing digital signal processing algorithms in hearing aids for low power consumption.

2. ADDER TOPOLOGIES

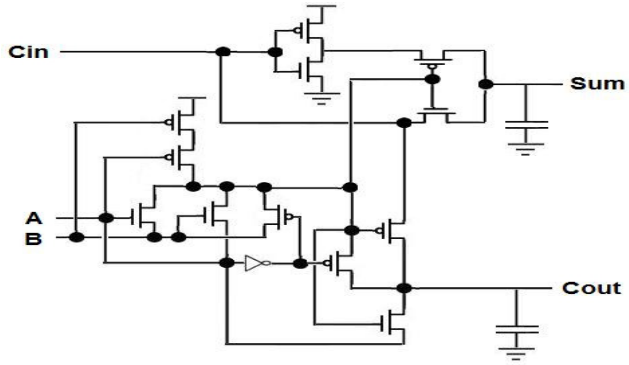
Most adder topologies are based on two XOR gates and one MUX. In [7] [10], [11.],different circuit topologies have been analyzed and simulated in different ranges of supply voltages. One of the most well known full adders is the standard static CMOS full adder that uses 28 transistors. In [4] the sense energy recovery full adder (SERF) is presented. The topology of this circuit is shown in Fig.c which requires only 10 transistors to implement it. In [12] different full adder topologies with a low number of transistors are presented.



(a) C-CMOS Full Adder [10]



(b) SERF Full Adder Architecture



(c) Modified SERF full adder

A. Multi-Operand Addition (> 2)

To avoid chaining of adders and to calculate the sum of multiple operands, two methods are in use.1. Adder arrays 2. Adder trees. Adder arrays are constructed as a linear arrangement of either carry-propagate (CPA) or carry-save adders (CSA). In the latter case, a carry propagate adder is used to merge the carry and sum vectors. The fastest implementation is achieved by an array of CSAs followed by a fast CPA. Array adders have a more regular structure and lower interconnection, but lower performance when compared to adder trees. Adder trees are constructed by a tree arrangement of compressors followed again by a carry propagate adder. In this way carry propagation is only performed once and postponed until after the tree. Effectively, addition is performed in carry-save format and the final carry-propagate can be perceived as a conversion layer between the carry-save and the standard 2's complement number representation. An adder tree made of full-adders is commonly known as a wallace tree [1].

B. Compressors for high-speed arithmetic circuits

Multiplexor (MUX) is used extensively in the digital design, for the efficient design of arithmetic and logic circuits. The CMOS implementation of MUX [22], performs better in terms of power and delay compared to exclusive-OR (XOR). Suppose, *X* and *Y* are inputs to the XOR gate, the output is $X\overline{Y} + \overline{X}Y$. The same XOR can be implemented using MUX with inputs *X;X* and select bit *Y* Efficient compressors have been designed using MUX. In the proposed compressors, both output and its complement of these gates are used.

1) Description of Compressors

A (*p;* 2) compressor has *p* inputs *X*1*;X*2 *: : :Xp*−1*;Xp* and two output bits (i.e., Sum bit and Carry bit) along with carry input bits and carry output bits. A full-adder is effectively a (3,2) compressor that encodes three input bits to two. A (4,2) achieves a higher compression rate and timing performance for the same area. For this reason it should be preferred for the construction of high fanin trees or the design of larger compressors. A (5*;* 2) compressor takes 5 inputs and 2 carry inputs and a (7*;* 2) compressor takes 7 inputs and 2 carry inputs. Block diagrams of these compressors are shown in Fig. 1.

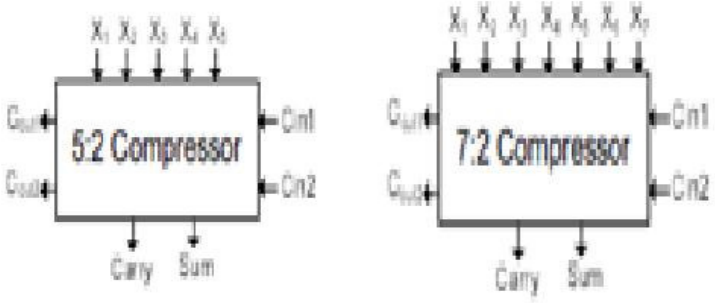


Fig. 1: Compressors (5:2,7:2)

Efficient designs of the existing XOR-based 5:2 and 7:2 compressors have critical path delays of 4Δ(*XOR*) and 6Δ(*XOR*) (delay denoted by Δ), respectively.

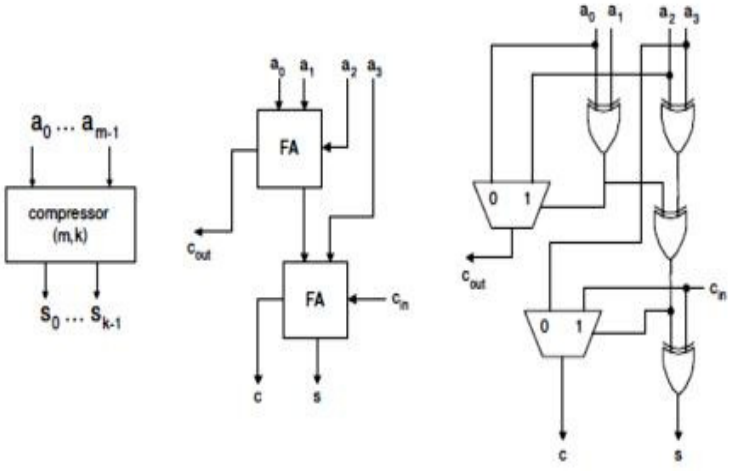


Fig. 2: 4:2 Compressor using FA

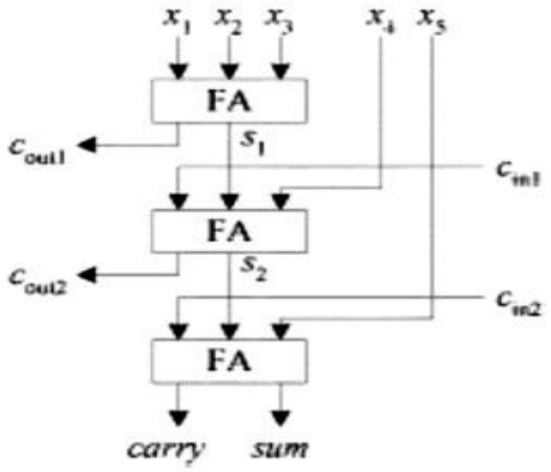


Fig. 3: 5:2 compressor using FA

C. 5-2 Compressor Architecture

The 5-2 compressor is another widely used building block for high precision and high speed multipliers. The block diagram of a 5-2 compressor is shown in, Fig 4 which has seven inputs and four outputs. Five of the inputs are the primary inputs X1,X2,X3,X4,X5and CIN1,CIN2 the other two inputs, and receive their values from the neighboring compressor of one binary bit order lower in significance. All the seven inputs have the same weight. The 5-2 compressor generates an output SUM of the same weight as the inputs, and three outputs CARRY,COUT1, COUT2 weighted one binary bit order higher. The outputs COUT1,COUT2, are fed to the neighboring compressor of higher significance.

D. Multipliers

A fast array or tree multiplier is typically composed of three subcircuits: a Booth encoder for the generation of a reduced number of partial products; a carry save structured accumulator for a further reduction of the partial products' matrix to only the addition of two operands; and a fast carry propagation adder (CPA) [9] for the computation of the final binary result from its stored carry representation. Among these subcircuits, the second stage of partial product accumulation, often referred to as the carry save adder (CSA) tree [1], [13],occupies a high fraction of silicon area, contributes most to the overall delay, and consumes significant power. Therefore, speeding up the CSA circuit and lowering its power dissipation are crucial to sustain the performance of the multiplier to stay competitive. To lower the latency of the partial product accumulation stage, 4-2 and 5-2 compressors have been widely used for high speed multipliers. Replacing an adder array with a Wallace adder tree results in aWallace multiplier and modified Wallace tree is shown in Fig 5.

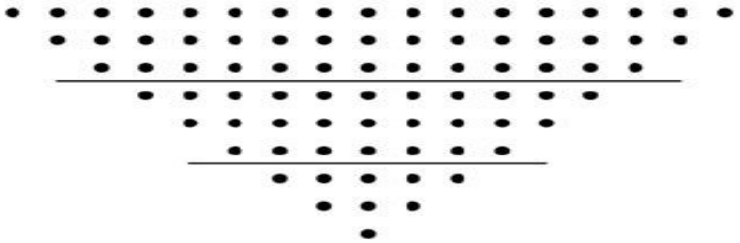


Fig. 4: Modified Wallace tree

3. PROPOSED SERF FULL ADDER

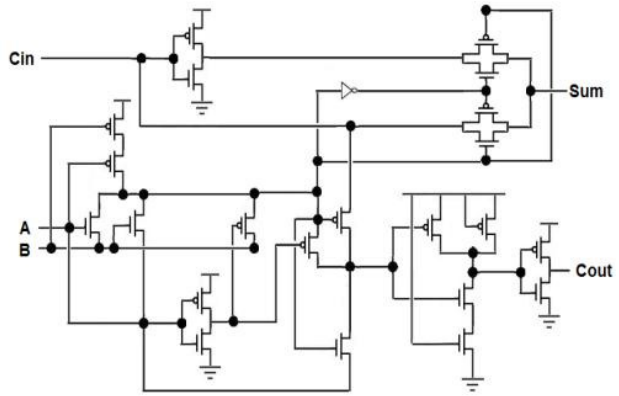


Fig. 5: Proposed FA based on SERF

The proposed Low power Full adder (Fig 5) uses the Novel XNOR circuit and the Transmission Gate based MUX along with level restoring clock gating technique for its operation. It is based on the Energy Recovery Concept [2]. By using Clock Gating Technique [14] the Carry out signal strength can be restored and also the use of AND gate which is one the most popular Low power Technique will reduce the power dissipation.

The gates of the pass transistors are connected to V_{DD} instead of V_{DD}-V_{th}, thus the power dissipating path is removed due to the completely turned-off PMOS transistors, which makes the output to rise till V_{DD}-V_{th} from of V_{DD} -2V_{th} [2], limiting the driving capability of the circuit. This reduction in output voltage (threshold voltage drop problem) makes cascading of pass transistor circuits difficult. And the use of such adder circuits in Compressors, Carry Propagation adders and Multiplier would lead to incorrect results. In the proposed design the Transmission Gate multiplexer is used so as to ensure full voltage swing at the sum output which will compensate for the loss of V_t. For input pulses of A=200MHz, B=100MHz and Cin=50MHz at 1.1V V_{DD}, the modified serf FA (Fig 7) showed power dissipation of 58.65µW and a delay of 7.05nS, whereas the proposed FA recorded power dissipation of 23.99µW and a delay of 6.09nS

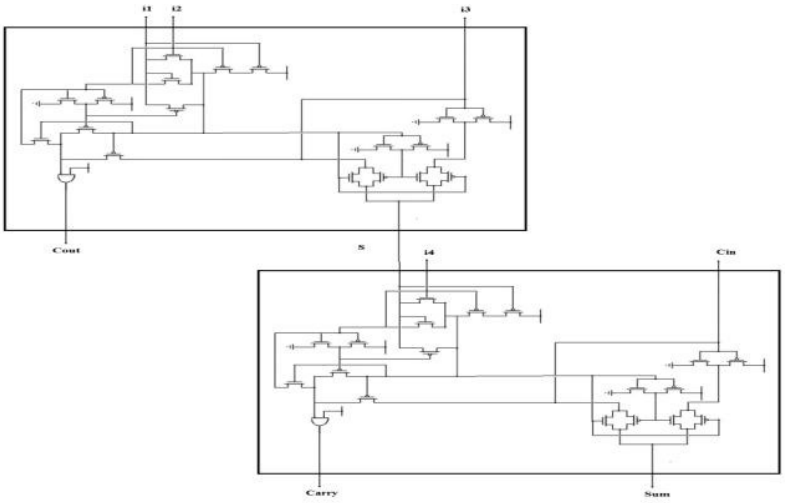


Fig. 6: 4:2 Compressor with proposed FA

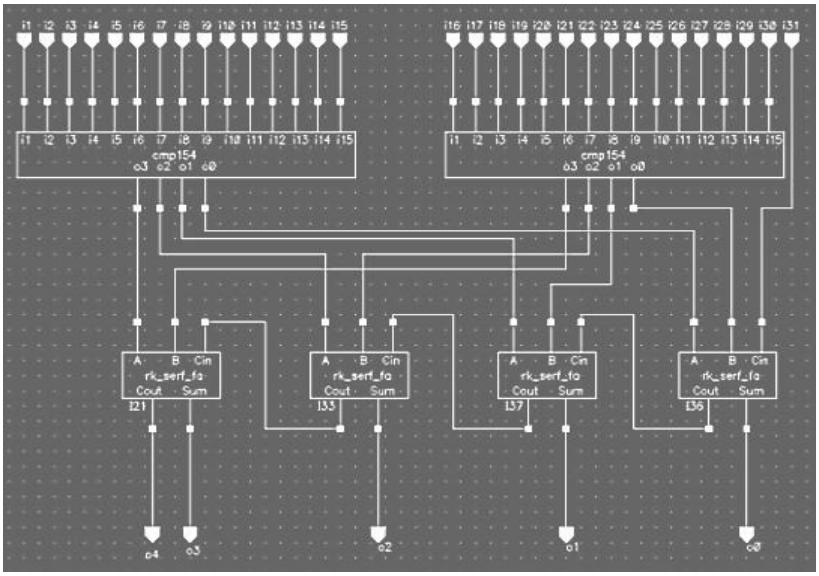


Fig. 7: 31: 5 compressor using lower level compressors

The compressors 11:2, 15:2, 31:2 which can be used in MAC units of DSP circuits are realized using the proposed full adder structure. The compressors speed up the addition process of partial products generate in a multiplier in turn reducing the delay and the adder used

Table I: PDP Full Adders (VDD =1.1V) CMOS 90nm Technology

FA Design	*Power Delay Product (fJ)*			
	5MHz	*50MHz*	*100MHz*	*200MHz*
C-CMOS	1403.100	221.8373	164.4129	144.8854
O-TGA	217.4269	174.5949	185.4085	212.7918
MBA-12T	05.60061	0.282211	0.25088	0.105492
ULPFA	263.4342	202.7862	217.5503	247.5988
Mfd SERF	6778.766	738.1514	398.0437	194.7882
Proposed FA	119.4373	048.9646	51.2313	054.7741

reduces the power dissipation due to AND operation used which is a kind of low power technique for power optimization.

4. SIMULATION RESULTS AND DISCUSSION

The Circuit Simulation works were carried out using numerous random input vectors with SPECTRE simulator in CADENCE VIRTUOSO Analog Design Environment under CADENCE CMOS 180nm and 90nm Technology respectively. The Power-delay product of the various full adder designs are listed in the Table I for comparison. The

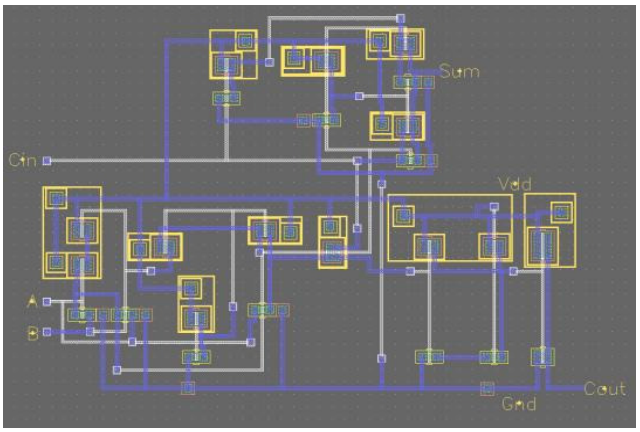


Fig. 8: Proposed adder layout

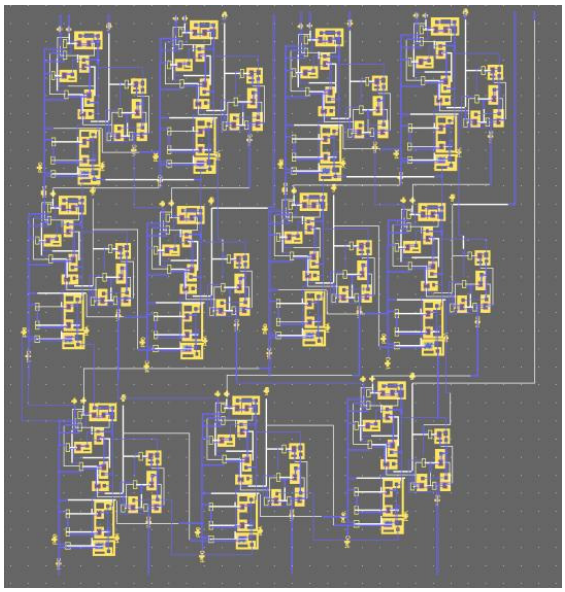


Fig. 9: 15:4 compressor Layout

layouts for all the adders and compressors were drawn using LAYOUT XL of CADENCE and DRC,LVS were run using ASSURA, RC parasites were extracted. In order to establish an impartial simulation environment, we preferred to give various input patterns as which covers every possible input combination of A, B, and C_{in}.

5. CONCLUSION

In this paper, we proposed a 24-transistor full-adder operating at 1.1 V power supply. The performance of various full-adders were compared and the simulation results proved that the proposed full-adder dissipate the lowest power consumption and has lowest PDP (Power Delay Product) and they can be used as a building block in compressor, multiplier and multiple and accumulate units that are used in hand held devices like Digital hearing aids which frequently employ the concept of filter banks. One of the major drawbacks of these techniques is the complexity of computation requiring more number of multiplications incresing the power consumption. Therefore the proposed multiplier architectures can be used as a new approach to speech enhancement for the hearing impaired and also the construction of filter bank in Digital hearing aid with minimum number of multiplications.

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