LOW POWER-AREA GDI & PTL TECHNIQUES BASED FULL ADDER DESIGNS

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ABSTRACT

Full adder circuit is functional building block of micro processors, digital signal processors or any ALUs. In this paper leakage power is reduced by using less number of transistors with the techniques like GDI (Gate Diffusion Input) and PTL (Pass Transistor Logic) techniques. In this paper 3 designs have been proposed of low power 1 bit full adder circuit with 10Transistors (using PTL multiplexer) , 8 Transistor
(by using NMOS and PMOS PTL devices), 12Transistors (6Transistors to generate carry using GDI technique and 6Transistors to generate sum using tri state inverters).

These circuits consume less power with maximum of 73% power saving com-pare to conventional 28T design. The proposed circuit exploits the advantage of GDI technique and pass transistor logic, and sum is generated by tri state inverter logic in all designs.

The entire simulations have been done on 180nm single n-well CMOS bulk technology, in virtuoso platform of cadence tool with the supply voltage 1.8V and frequency of 100MHz.

KEYWORDS

leakage power, GDI, Pass transistor logic, tri-state inverters.

1. INTRODUCTION

As the applications requiring low power and high performance circuits increasing, this has intensified the research effort in low power microelectronics. Full adder circuit is functional building block and most critical component of complex arithmetic circuits like micro processors, digital signal processors or any ALUs [1]. Almost every complex computational circuit requires

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full adder circuitry. The en-tire computational block power consumption can be reduced by implementing low power techniques on full adder circuitry.

Several full adder circuits have been proposed targeting on design accents such as power, delay and area. Among those designs with less transistor count using pass transistor logic have been widely used to reduce power consumption [2-4]. In spite of the circuit simplicity, these designs suffer from severe output signal degradation and cannot sustain low voltage operations [5].

In these designs we have exploited the advantages of GDI technique and PTL technique for low power. In these designs, we have generated carry using GDI technique, we have generated carry using PMOS and NMOS pass transistors and also by using modified multiplexer using pass transistors. The motivation is to use the tri-state inverter instead of inverter as it reduces power consumption by 80% when compare to normal inverter. And sum is generated using 6T XOR module as shown in Fig.7.

The rest of the paper is organised as previous research work, proposed full adder designs, simulations-results-comparison and conclusion.

2. PREVIOUS WORK

Many full adder designs have been reported using static and dynamic styles in papers [1-4]. These designs can be divided into two types, the CMOS logic and the pass-transistor logic [5]. Different full adder topologies have been proposed using standard XOR and XNOR circuits and with 3T XOR-XNOR modules.

In [5] a low power full adder cell has been proposed, each of its XOR and XNOR gates has 3 transistors. Advantages of pass-transistor logic and domino logic encouraged researchers to design full adder cell using these concepts [6] [7]. Full adder cells based on Sense energy recovery full adder (SERF) [8] and Gate diffusion input (GDI) techniques [5] are common. To attain low power and high speed in full adder circuits, pseudo-NMOS style with inverters has been used [9]. A 10 transistors full adder using top-down approach [10] and hybrid full adder [11] are the other structures of full adder cells. Sub threshold 1-Bit full adder cell and hybrid CMOS design style are the other techniques that targeted on fast carry generation and low PDP.

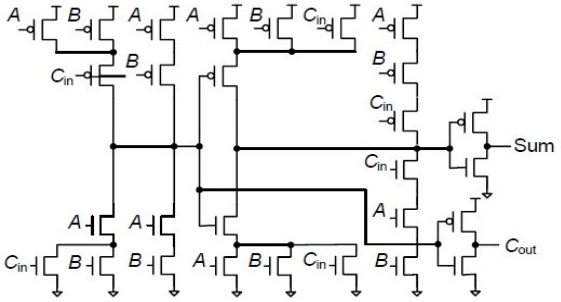

Fig 1. conventional 28T full adder

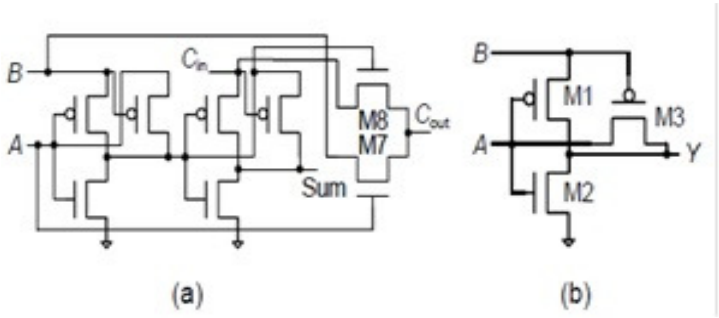

Fig 2. Design of chowdhury etal.(2008) (a) 8T full adder, (b) 3T XOr gate

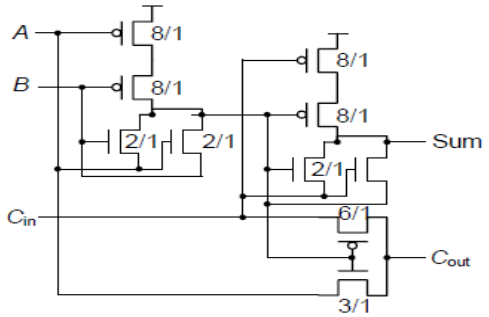

Fig. . 3. SERF full adder design

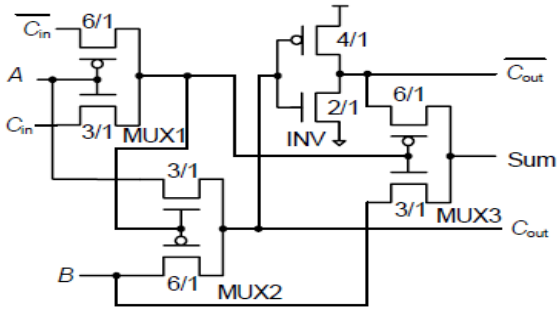

Fig. 4. 8T full adder design [17].

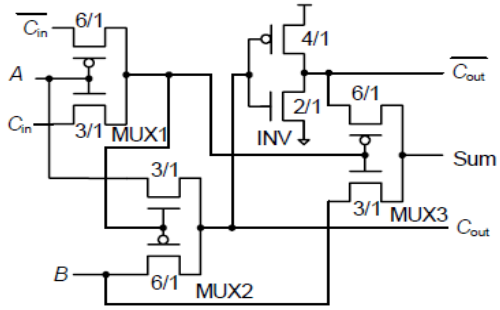

Fig. .5 8T full adder design [18]

3. DESIGN OF PROPOSED FULL ADDER CIRCUITS

1 3T XOR gate and tri-state inverter design

Most full adder designs with less transistor count adopt 3-module implementations i.e.XOR (or XNOR), for sum as well as carry modules [1]. For PTL based designs, it requires at least 4 transistors to implement a XOR (or XNOR) module [5, 8] but the design faces severe threshold voltage loss problems.

The motivation for these designs is use of tri-state inverter instead of normal inverter because tri-state inverter's power consumption is 80% less than normal inverter. In normal inverter the supply voltage is always HIGH; while in the tri-state inverter the supply voltage is not always HIGH. This reduces the average leakage of the circuit throughout operation. The diagram for tri-state inverter is shown on Fig. 6.

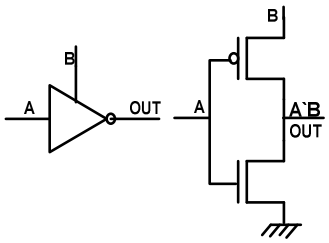

Fig. 6 Tristate inverter.

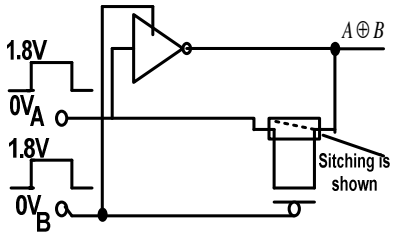

Fig 7. 3T XOR module

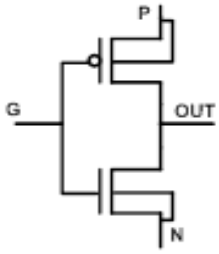

Fig 8. Basic GDI cell

Switching of the MOS transistor is also shown in fig. 7 and it is repeated in all figures.

2 Proposed 12T full adder design

The proposed 12T full adder design incorporates the 3T XOR module made by tri-state inverter as shown in Fig.7. The design follows with the conventional 2 module implementation of 3 input XOR gate, this facilitate sum module of the full adder.

The modified equations (1) for 12T full adder design are:

$$
\begin{aligned}
&sum = a \oplus b \oplus c \\
&\Rightarrow (a \oplus b) \oplus c \\
&carry = ab + bc + ca \\
&ab + bc + ca = ab + bc(a + a`) + ac(b + b`) \\
&\Rightarrow ab + abc + a`bc + ab`c \\
&\Rightarrow ab(1 + c) + (a`b + ab`)c \\
&\Rightarrow ab + (a \oplus b)c
\end{aligned}
\qquad (1)
$$

The sum is generated by implementing 3T XOR module twice. Carry module is generated here by using GDI technique.

The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced

number of transistors (as compared to CMOS and existing PTL techniques), while improving logic level swing and static power characteristics.

1) The GDI cell contains three inputs G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS).

2) Body of both nMOS and pMOS are connected to N or P (respectively) as shown in Fig.8. , so it can be arbitrarily biased at contrast with a CMOS inverter.

This circuit exploits the low power advantages of GDI circuits to generate carry and tri-state inverter for generating sum. The equations have modified as above to generate carry. Basic operations like AND, OR have performed using GDI technique to generate carry, for example in the equation (1) $a.b$ and $(a \oplus b)c$ have been performed using GDI and gates. Sum is implemented by using 3T (XOR) module twice as shown in Fig.9.

3 Proposed 10T full adder design:

The proposed 10T full adder uses the concept of pass transistor logic based multiplexer. The pass transistor design reduces the parasitic capacitances and results in fast circuits. The multiplexer is implemented using pass transistors for carry generation. This design is simple and efficient in terms of area and timing. The proposed 10T full adder circuit can be visualised by modifying the equations (2) as accordingly

The modified equations for 10T full adder design:

$$\begin{aligned} &sum = a \oplus b \oplus c \\ &\Rightarrow (a \oplus b) \oplus c \\ &carry = ab + bc + ca \\ &\Rightarrow ab + (a \oplus b)c \\ &\Rightarrow ab(a \oplus b)` + (a \oplus b)c \end{aligned} \qquad (2)$$

The multiplexer using pass transistor logic can be visualised in 2T model, the select signal for the multiplexer here is ($a \oplus b$). The equations have modified such that select signal is in the form of ($a \oplus b$). The ($a.b$) signal is generated by using the tri-state inverter for

$$(a`b) \Rightarrow (a`b)`b = (a + b`).b \Rightarrow a.b + b.b` \Rightarrow a.b \qquad (3)$$

The sum is generated by implementing 3T XOR module twice. Carry is generated by using pass transistor logic based multiplexer whose select line is ($a \oplus b$) as shown in Fig.10.

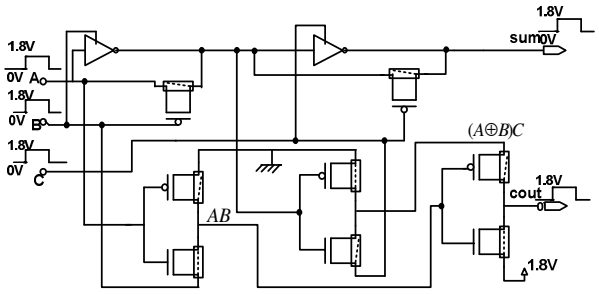

Fig. .9. proposed 12T full adder design

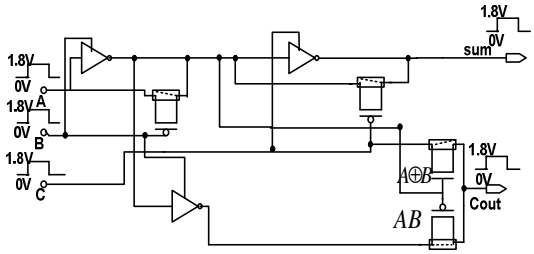

Fig. 10. proposed 10T full adder design

4 Proposed 8T full adder design:

In the proposed 8T full adder sum is generated using 3T XOR module twice, and carry is generated using NMOS and PMOS pass transistor logic devices as shown in Fig.11. The equations (4) are modified so as to visualise the 8T full adder design.
The modified equations for 8T full adder design are:

$$\begin{aligned} &sum = a \oplus b \oplus c \\ &\Rightarrow (a \oplus b) \oplus c \\ &carry = ab + bc + ca \\ &\Rightarrow ab + bc(a + a`) + ac(b + b`) \\ &\Rightarrow ab + (a \oplus b)c \\ &\Rightarrow (a`b)`b + (a \oplus b)c \end{aligned} \tag{4}$$

In this design instead of using two NMOS pass transistor devices we have used one NMOS and one PMOS pass transistor device, because of ease of the design and as according to the equation as shown in Fig.11.

It must be noted that PMOS transistor passes ' 1' very good, but cannot pass '0' completely thus, the carry output has weak '0'. NMOS transistor passes '0' very good, but cannot pass '1' completely therefore, the carry output has weak ' 1 ', Having weak '0' and '1' at carry outputs is one of the disadvantages of proposed 8T full adder circuit. In practical situations, this problem can be solved by using an inverter at carry output, but this solution leads to increased power and area.

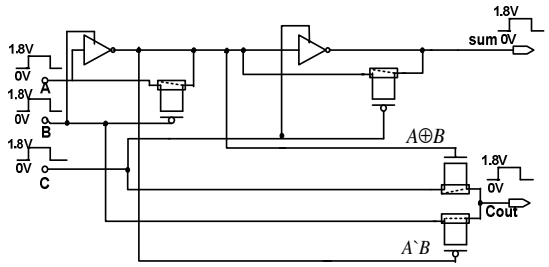

Fig 11. Proposed 8T full adder design

4. SIMULATION RESULTS AND COMPARISON

The entire simulations have been done on 180nm single n-well CMOS bulk technology, in virtuoso platform of cadence tool with the supply voltage 1.8V and frequency of 100MHz. The entire results are compared with the different techniques. Area is calculated by using micro wind software. The area is reduced by 48% for proposed 12T design, the area is reduced by 66% for proposed 8T design and area is reduced by 53% when compared to 28T conventional full adder design.

Table 1 Simulation Results

Full Adder Designs	Conventional(28T)	Chowdury deign(8T)	8T(ref .15)	8T(ref .16)	SERF	Proposed (12T)	Proposed (8T)	Proposed (10T)
Min supply voltage(V)	1.8	1.8	1.8	1.6	1.6	1.6	1.6	1.4
Cout delay (nS)	0.366	0.513	0.496	0.5	0.39	0.476	0.502	0.512
Avg.power consumption (uW)	52.4	17.4	36.47	27.7	18.2	14.3	16.0	17.1
Number-of transistors	28	8	8	8	10	12	8	10
Power* Delay (uW.nS)	19.178	8.926	18.08	12.6	7.09	6.806	8.032	8.755

5. CONCLUSION

Three new full adder designs have been proposed and simulation results have been compared with the previous results in umc180nm technology using cadence tool. According to the

simulation results the power consumption has been improved maximum by 73% when proposed circuits are compared to conventional 28T adder and other reference circuits.

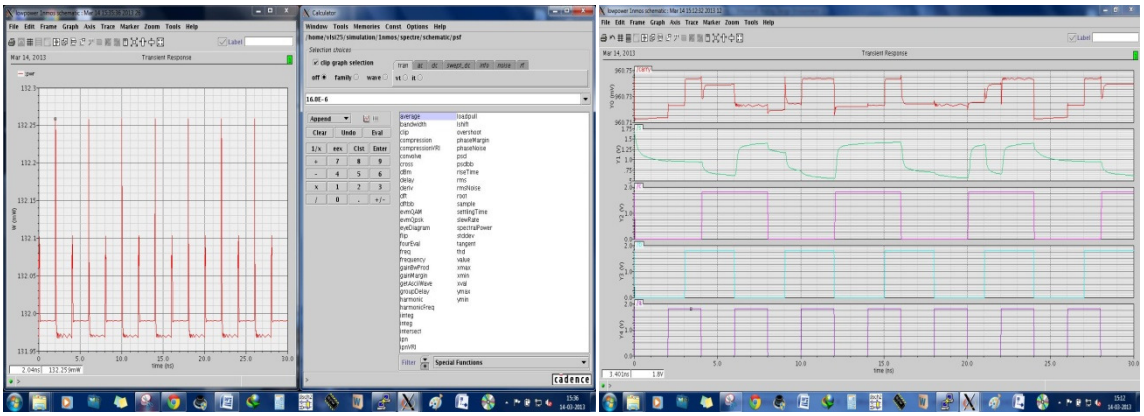

Fig. .12. Simulation results and power waveform of Proposed 8T full adder

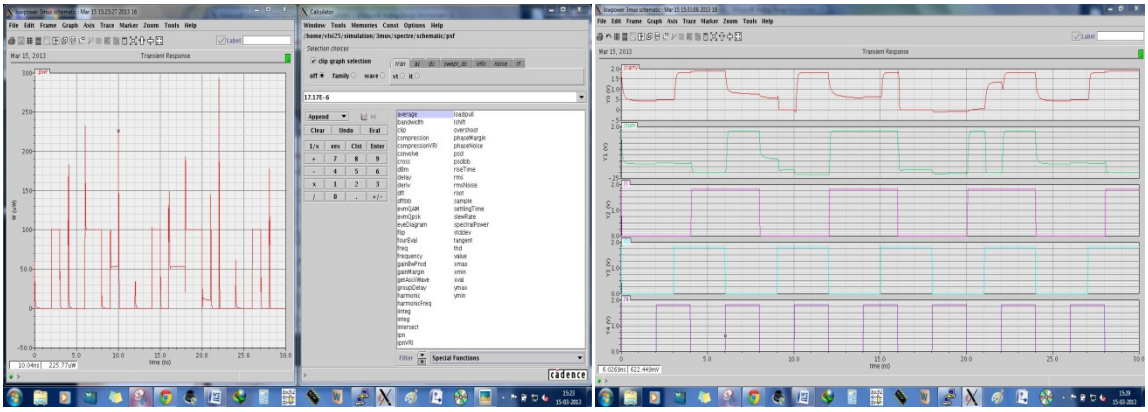

Fig. .13. Simulation results and power waveform of Proposed 10T full adder design

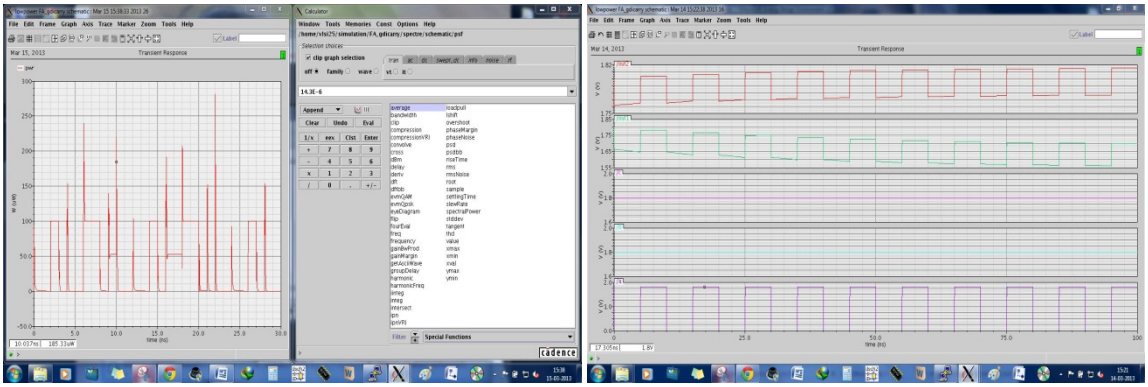

Fig. .14. Simulation results and power waveform of Proposed 12T full adder design

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