SEMI ADIABATIC ECRL AND PFAL FULL ADDER

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ABSTRACT

Market demands have compelled the VLSI industry stake holders to integrate more and more number of functionalities and which is also being well supported by the advances in fabrication techniques. This has challenged the circuit designers to design the power ware circuits and in the process many experts are using concept from other engineering areas to resolve the power equations more optimally. Adiabatic Logic is one such technique used to reduce the power dissipation of the circuit utilizing the principle from thermo dynamic of zero entropy exchange with environment. Authors have used adiabatic principle and implemented full adder circuit with ECRL and PFAL techniques. Transistor count for carry and sum are 14, 22 and 16, 24 respectively for ECRL and PFAL. The maximum frequency, maximum load driving capability are analyzed for 1.25 micron and 0.18 micron technology. It is found that for 1.25 micron technology ECRL based carry circuit dissipates least power of 2.860176 µW at 25 MHz, max power of 18.17460 µW at 100 MHz and maximum Cload derived is 7 fF with 8.464489 µW at 50 MHz. The PFAL based carry circuit dissipates least power of 38.52858 µW at 20 MHz, max power of 51.52832 µW at 100MHz and maximum Cload derived is 20 fF with 40.61746 µW at 50 MHz. ECRL based sum circuit dissipates least power of 4.932597 µW at 25 MHz, max power of 53.1588 µW at 100 MHz and maximum Cload derived is 30 fF with 29.6655 µW at 50 MHz. The PFAL based sum circuit dissipates least power of 7.052026 µW at 25 MHz, max power of 53.33038 µW at 100 MHz and maximum Cload derived is 20 fF with 24.11132 µW at 50 MHz. For 0.180 micron technology – ECRL based carry circuit dissipates 59.2158 µW at fmax of 200MHz and maximum Cload derived is 20 fF with 88.63479 µW at 200MHz. PFAL based carry circuit dissipates 583.6617 µW at 20 MHz. ECRL based sum circuit dissipates 24.37457 µW at fmax of 200 MHz and maximum Cload derived is 10 fF with 38.95504 µW at 200MHz. PFAL based sum circuit dissipates 1555.033 µW at 20 MHz.

KEYWORDS

ECRL, PFAL, Full Adder, Adiabatic circuit

1. INTRODUCTION

Low power circuits aim at providing best output and utilizing minimum possible power. Need for low power VLSI circuits is increasing day by day due to remarkable success and growth of the class of personal computing devices and wireless communications systems which demand high-speed computation and complex functionality with low power consumption. Large power

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dissipation requires larger heat sinks hence increased area and cost, and therefore highlight the need and importance of low power circuits.

Adiabatic Logic is based on adiabatic switching principle. The term 'adiabatic' refers to a process in which there is no heat exchange with the environment [8-10]. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy [1].

2. ADIABATIC LOGIC TYPES

Adiabatic families can be mainly classified as either Partially Adiabatic or Fully Adiabatic [2]. In Partially Adiabatic circuits, some charge is allowed to be transferred to the ground, while in Fully Adiabatic Circuits, all the charge on the load capacitance is recovered by the power supply.

Efficient Charge Recovery Logic (ECRL) and Positive Feedback Adiabatic Logic (PFAL) are partially adiabatic techniques. ECRL is based around a pair of cross-coupled PMOS transistors. Their source terminals are connected to the power-clock, and the gate of each one is connected to the drain of the other. These nodes form the complementary output signals. The function is evaluated by a series of pull-down NMOS devices [3]. The basic structure of ECRL circuits is shown in figure 1. The core of the PFAL circuits is a latch made by the two PMOS and two NMOS, that avoid a logic level degradation on the output nodes "*out*" and "*/out*". The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. Figure 2 shows the PFAL basic structure.

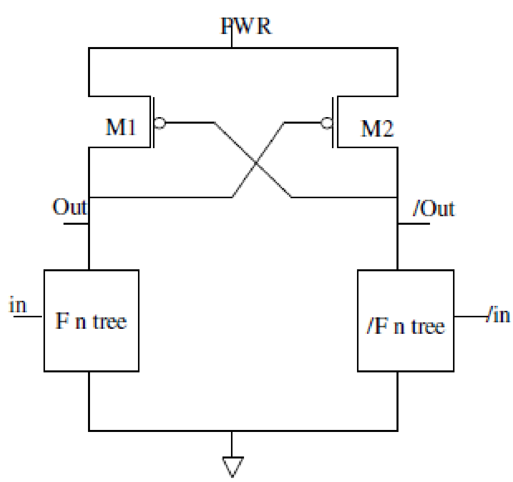

Fig 1: Basic structure of ECRL [3]

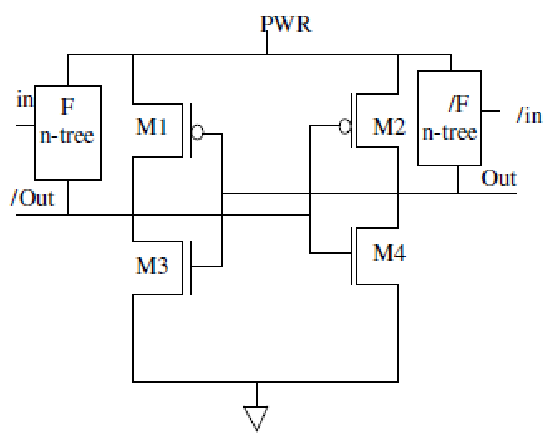

Fig 2: Basic structure of PFAL [4]

3. CIRCUIT IMPLEMENTATION

A 1-bit full adder is a basic cell in digital computing systems. If it has three 1-bit inputs (A, B, and C) and two 1-bit outputs (sum and carry), then the relations between the inputs and the outputs can be expressed as:

$$\mathrm{sum} = \overline{\mathrm{A}}(\,\overline{\mathrm{B}}\mathrm{C} + \mathrm{B}\overline{\mathrm{C}}\,) + \mathrm{A}(\,\overline{\mathrm{B}}\overline{\mathrm{C}} + \mathrm{BC})$$
$$\mathrm{carry} = \mathrm{AB} + \mathrm{BC} + \mathrm{CA}$$

Tanner ECAD tool [8] is used for implementing the ECRL and PFAL semi adiabatic, dual rail full adder circuit and results obtained from the two are compared. 1.25 micron and 0.18 micron technologies are used. Tanner suit components S-edit is used for schematic entry, TSpice for simulation and W-Edit for waveform analysis.

The logic function blocks (F) shown in the basic structures of ECRL and PFAL can be implemented using the above equations of sum and carry. Similarly, /F logic function block can be implemented by finding out the complement of sum and carry equations and then simplifying them. The equations for /F logic function block will be as follows:

$$\overline{\mathrm{sum}} = \mathrm{A}(\,\mathrm{B}\overline{\mathrm{C}} + \overline{\mathrm{B}}\mathrm{C}) + \overline{\mathrm{A}}(\,\mathrm{BC} + \overline{\mathrm{B}}\overline{\mathrm{C}})$$
$$\overline{carry} = (\bar{A} + \bar{B}).(\bar{B} + \bar{C}\,).(\bar{C} + \bar{A})$$

Figure 3 to figure 6 show the circuit implementations of the sum and carry using ECRL and PFAL techniques.

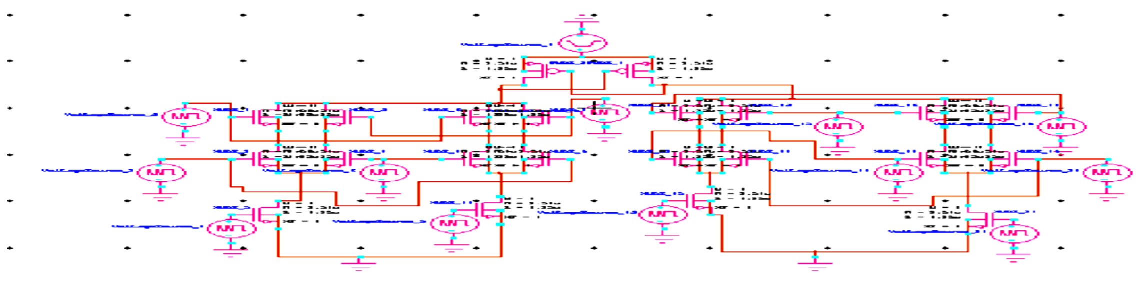

Fig 3: Circuit of Sum in an Adder using ECRL

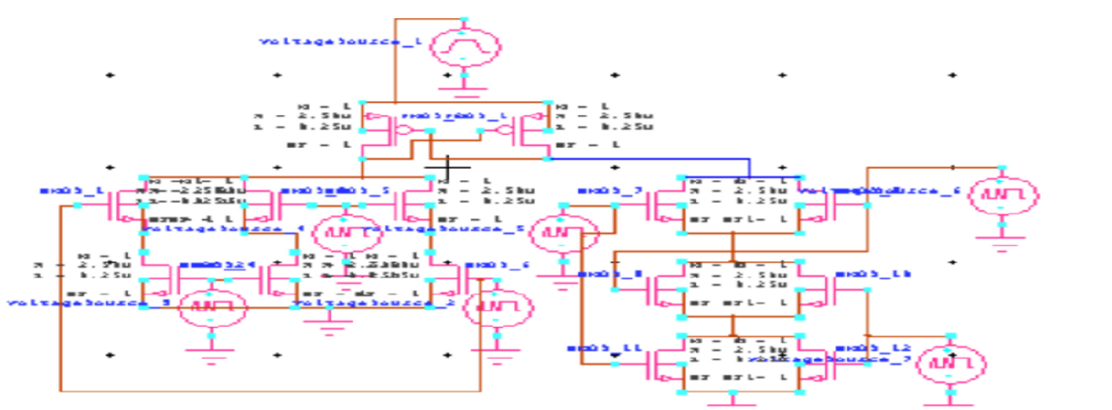

Fig 4: Circuit of Carry in an Adder using ECRL

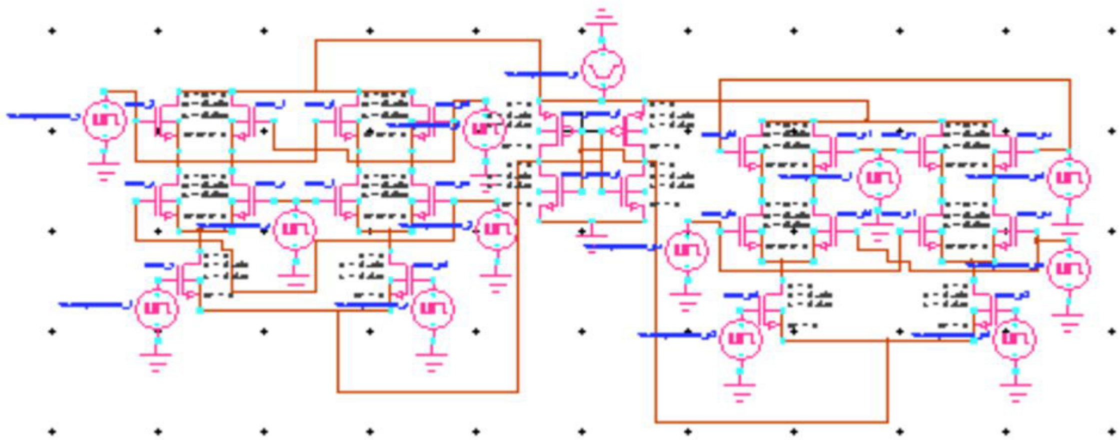

Fig 5: Circuit of Sum in an Adder using PFAL

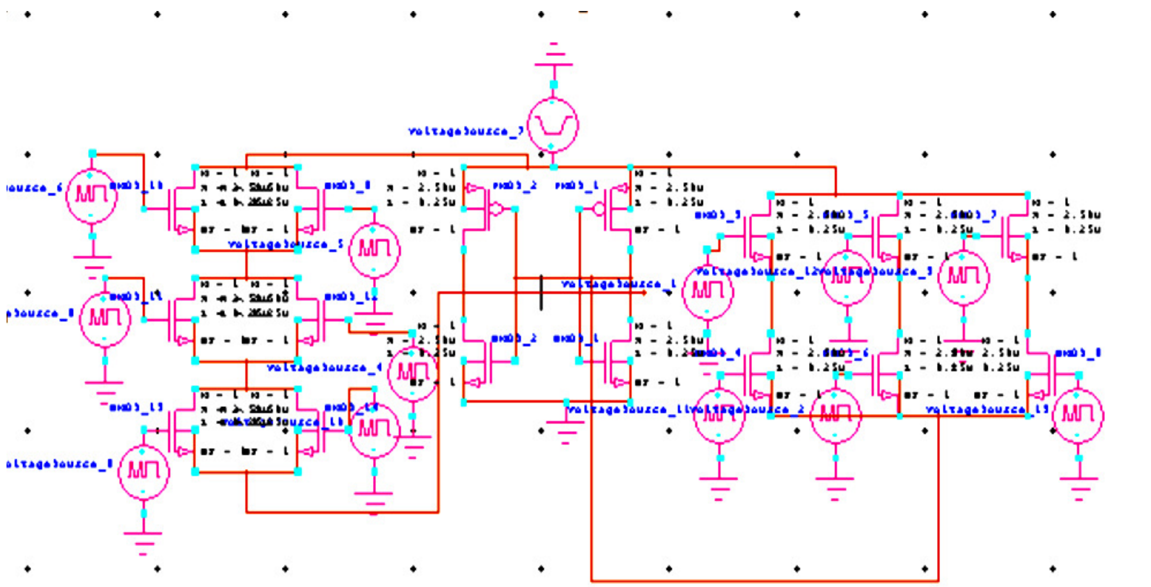

Fig 6: Circuit of Carry in an Adder using PFAL

4. RESULTS

The two circuits are verified with different set of test vectors covering several input combinations for different set of frequencies and load capacitances. The simulation waveforms are shown in figure 7 to figure 10. The results pertaining to minimum voltage, average power, maximum frequency and maximum load are tabulated in table1 to table 7. The results are graphically analyzed and shown in figure 11 to figure 17.

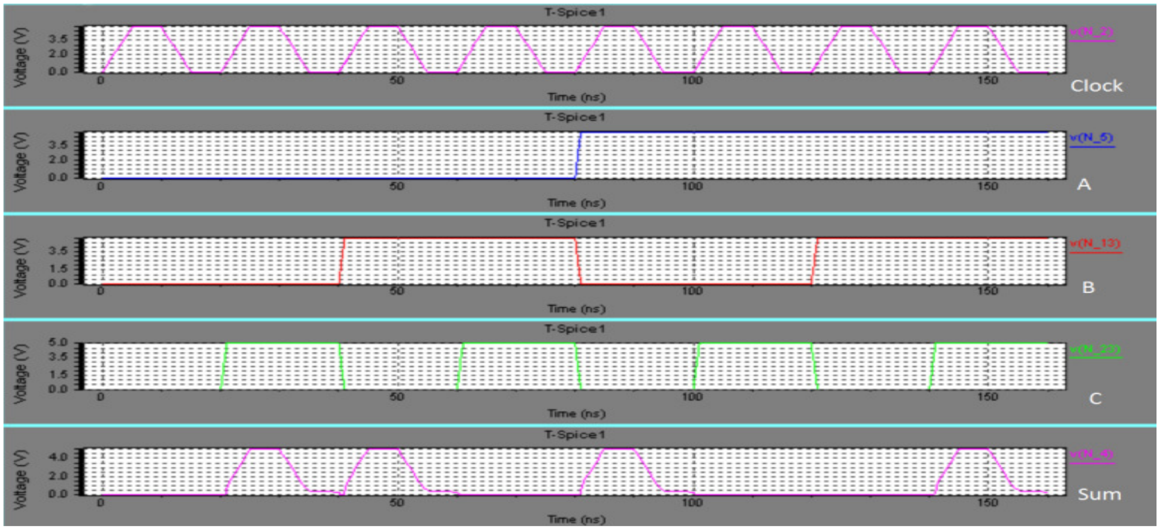

Fig 7: Waveform for Sum in an Adder using ECRL

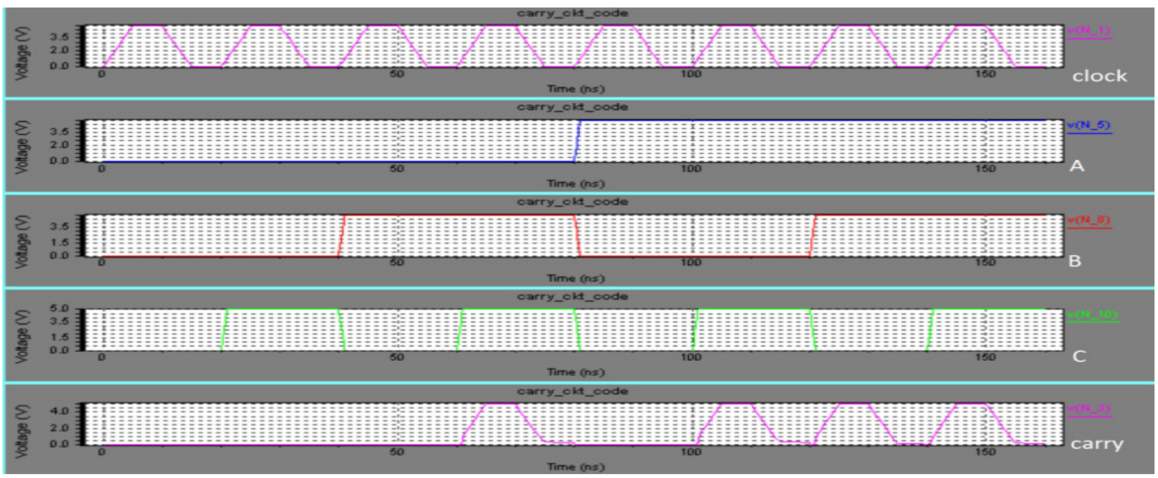

Fig 8: Waveform for Carry in an Adder using ECRL

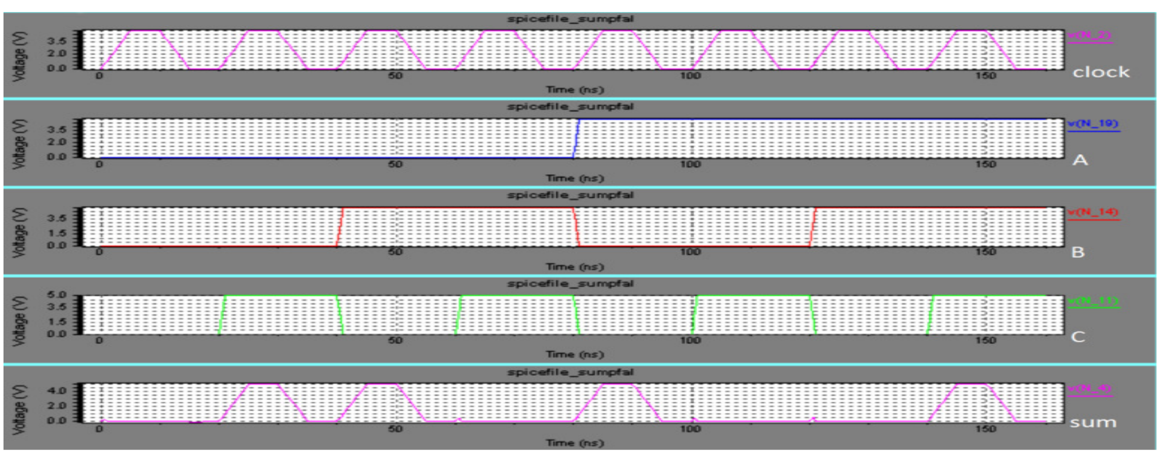

Fig 9: Waveform for Sum in an Adder using PFAL

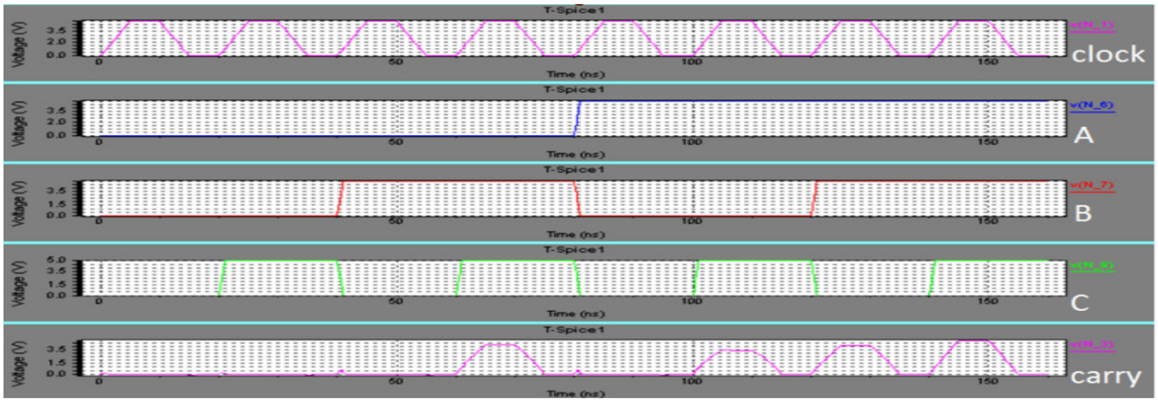

Fig 10: Waveform for Carry in an Adder using PFAL

Table 1: Results using ECRL for carry circuit using 1.25 micron technology

FREQUENCY(MHz)	AVERAGE POWER(μW)
25	2.860176
50	6.332866
100	18.17460

Table 2: Results using ECRL for sum circuit using 1.25 micron technology

FREQUENCY(MHz)	AVERAGE POWER(μW)
25	4.932597
50	16.04846
83.33	39.80059
100	53.1588

Table 3: Results using PFAL for carry circuit using 1.25 micron technology

FREQUENCY(MHz)	AVERAGE POWER(μW)
20	38.52858
25	37.75284
50	37.36084
100	51.52832

Table 4: Results using PFAL for sum circuit using 1.25 micron technology

FREQUENCY(MHz)	AVERAGE POWER(μW)
25	7.052026
50	21.73065
100	53.33038

Table 5: Results for Cload using 1.25 micron technology

CIRCUIT	FREQUENCY(MHz)	AVERAGE POWER(μW)	MAXIMUM LOAD CAPACITOR(fF)
Carry(ecrl)	50	8.464489	7
Sum(ecrl)	50	29.6655	30
Carry(pfal)	50	40.61746	20
Sum(pfal)	50	24.11132	20

Table 6: Transistor count, fmax and power results for sum and carry using 0.18 micron technology

CIRCUIT	NUMBER OF TRANSISTORS		MAXIMUM FREQUENCY(MHz)		AVERAGE POWER(μW)	
	ECRL	PFAL	ECRL	PFAL	ECRL	PFAL
Carry	14	16	200	20	59.2158	583.6617
Sum	22	24	200	20	24.37457	1555.033

Table 7: Cload and power results for sum and carry using 0.18 micron technology pertaining to fmax

CIRCUIT	MAXIMUM LOAD CAPACITOR(Ff)	AVERAGE POWER(μW)
ECRL(Carry)	20	88.63479
ECRL(Sum)	10	38.95504

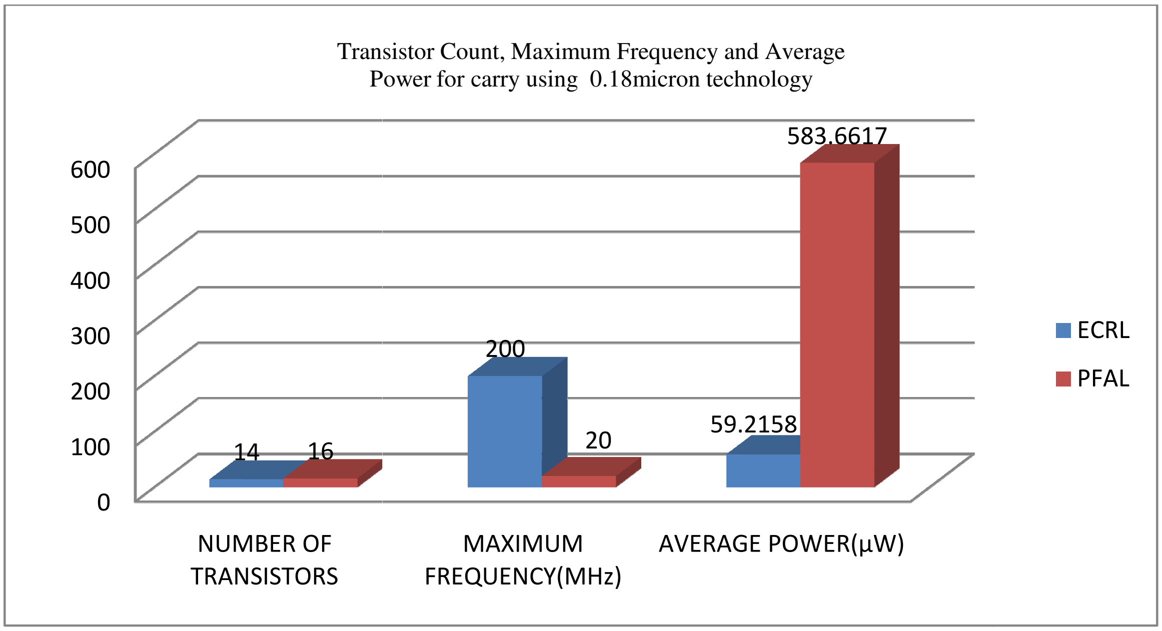

Fig 11: Comparison between carry-ECRL and PFAL for 0.18 micron technology

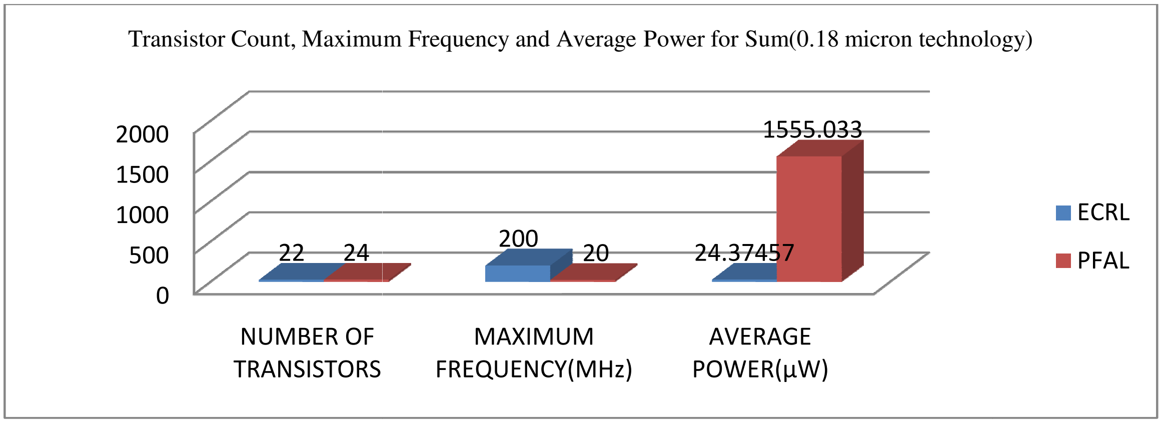

Fig 12: Comparison between sum-ECRL and PFAL for 0.18 micron technology

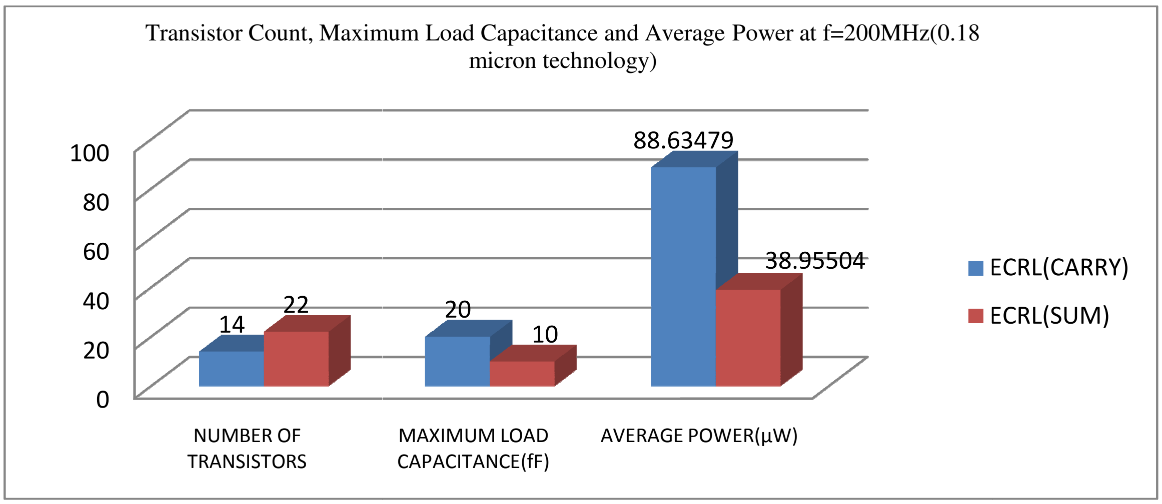

Fig 13: Transistor Count, Maximum Load Capacitance and Average Power at f=200MHz ECRL sum and carry for 0.18 micron technology

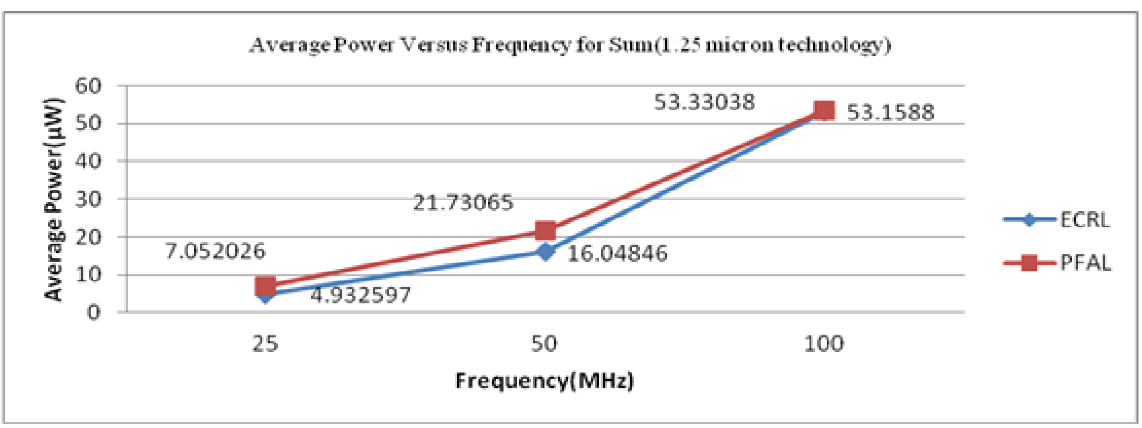

Fig 14: Average Power and Frequency for Sum ECRL and PFAL for 1.25 micron technology

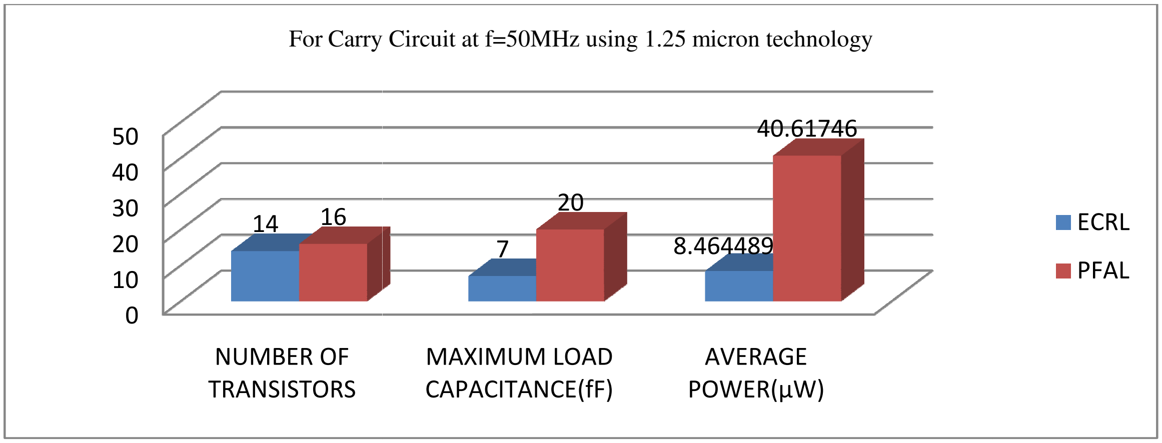

Fig 15: ECRL and PFAL Carry Circuit at f=50MHz using 1.25 micron technology

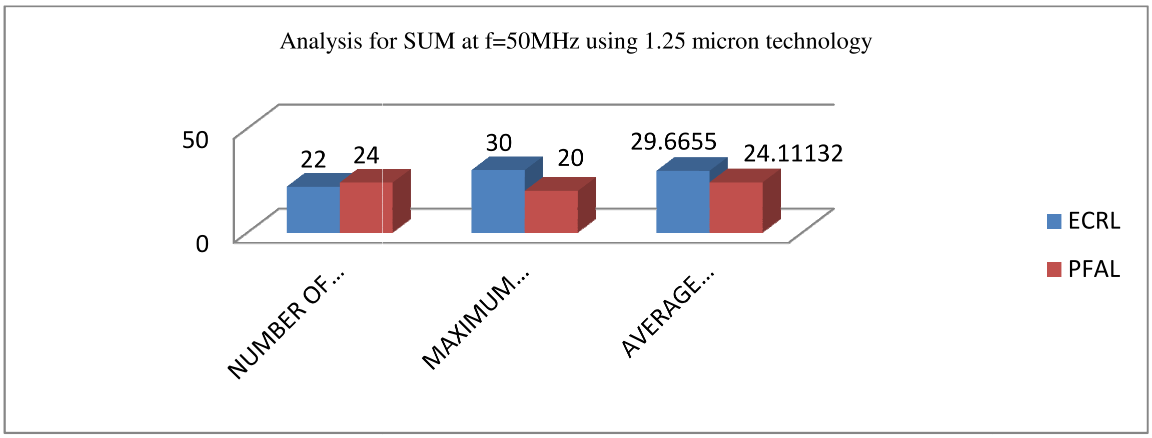

Fig 16: ECRL and PFAL Sum Circuit at f=50MHz using 1.25 micron technology

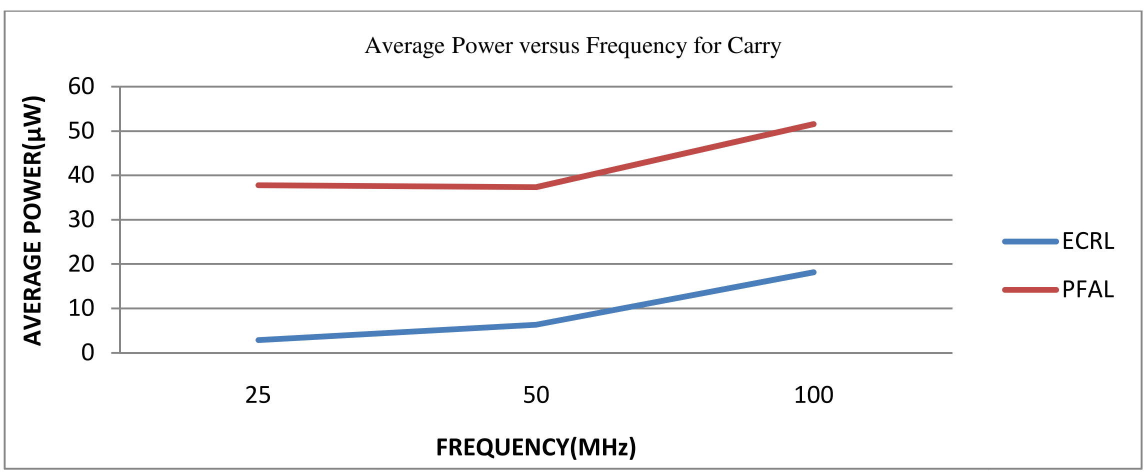

Fig 17: ECRL and PFAL Carry Circuit Power vs frequency

5. CONCLUSION

Authors have implemented the full adder circuit using semi adiabatic, dual rail, ECRL and PFAL techniques with 1.25 micron and 0.18 micron technology. Through the implementation, authors have compared the two techniques with respect to the transistor count, maximum operating frequency, power dissipation and output level quality. The transistor count for carry and sum are 14, 22 and 16, 24 respectively for ECRL and PFAL. It is found that for 1.25 micron technology ECRL based carry circuit dissipates least power of 2.860176 µW at 25 MHz, max power of 18.17460 µW at 100 MHz and maximum Cload derived is 7 fF with 8.464489 µW at 50 MHz. The PFAL based carry circuit dissipates least power of 38.52858 µW at 20 MHz, max power of 51.52832 µW at 100MHz and maximum Cload derived is 20 fF with 40.61746 µW at 50 MHz . ECRL based sum circuit dissipates least power of 4.932597 µW at 25 MHz, max power of 53.1588 µW at 100 MHz and maximum Cload derived is 30 fF with 29.6655 µW at 50 MHz. The PFAL based sum circuit dissipates least power of 7.052026 µW at 25 MHz, max power of 53.33038 µW at 100 MHz and maximum Cload derived is 20 fF with 24.11132 µW at 50 MHz. For 0.180 micron technology – ECRL based carry circuit dissipates 59.2158 µW at fmax of 200 MHz and maximum Cload derived is 20 fF with 88.63479 µW at 200MHz. PFAL based carry circuit dissipates 583.6617 µW at 20 MHz. ECRL based sum circuit dissipates 24.37457 µW at fmax of 200 MHz and maximum Cload derived is 10 fF with 38.95504 µW at 200MHz. PFAL based sum circuit dissipates 1555.033 µW at 20 MHz. The output levels for PFAL are better and stabilize quickly as compared to the ECRL based full adder circuit.

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