SCAN CHAINS TESTING FOR LATCHES TO REDUCE AREA AND THE POWER CONSUMPTION

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ABSTRACT

During the test mode of flip flop in a chip, a set of input vectors are sent through the flip-flop, it consumes more power consumption than in the normal functional mode. In this paper, we propose a latch with bi -stable element which reduces area as well as the power consumed. The latch proposed consists of simple basic gates involving two inverters back to back which acts as a bi-stable element and a transmission gate with the clock signal used to enable and disable the rest of the circuit with impact on running the latch on Static Timing Analysis. The input test vectors are either given by Automatic Test Pattern Generation (ATPG) or many other methods. We model this using T-Simulation Program with Integrated Circuit Emphasis (T-SPICE) and see the power consumed.
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KEYWORDS

Scan Chain, Latch, Bi-stable element, ATPG, Flip-Flops

1. INTRODUCTION

As the scale of integration improves, more number of transistors, faster and smaller than their predecessors are being packed into a chip. This leads to steady growth of the operating frequency and processing capacity per chip, resulting in increased power dissipation. The power consumption of a high performance Micro-processor is now approaching several dozen Watts. Sequential circuits are usually designed with flip flops or latches. These are sometimes called memory elements, used to store a single bit [1]. The applied test vectors can be applied either by ATPG or even manually.
Power Dissipation can be Dynamic power dissipation and Static power dissipation. Static power dissipation is related to the logical states of the circuits. Dynamic power dissipation is caused by switching activities. Since dynamic power is major in CMOS design so we go for analysis and reduction in number of gates.

2. Related Works

Proposed works which have already been done are using Gating [3] and holding the output values of the element, works on scan architecture which divides the scan chain and activates only when it is performed for that particular instance [4], modified scan flip flop which involves disabling

the slave latch [5] which reduces the power by disabling the slave when it is in the scan mode without any extra circuitry.

Here we just propose a simple latch, that eliminates the power consumed and the number of gates when compared to a normal flip flop, area during testing and also this reduces the gate delay. The data which comes from a ATPG is given and the scan is got at the output with the switching activity involved because of only inverters. This latch can also work on the operating frequency of the chip or even lesser frequency.

2.1. Contribution of the Paper

The papers work is done as follows: (A)First we consider a normal D-flip flop and a D-Latch see the gate area, the number of gates and the area consumed. (B) Then we consider the propsed latch and run it at different frequency and see if the results are tallied. (C) Then we compare the two results with respect to area and the power consumed and see which is the better among the three. We discuss in section 3 the proposed model and the advantages over the existing designs. In section 4 we discuss the results.

3. Proposed Model

A D-Latch which has an enable input as shown in Figure 1. When the Enable signal is set to 1, the Q output is same as theD input. The latch is said to be "open" and the path from the input D to the output Q is transparent. Hence the circuit is often referred to as a transparent latch. When E is de-asserted , the latch is disabled or "closed", and the Q output retains its last value independent of the D input.
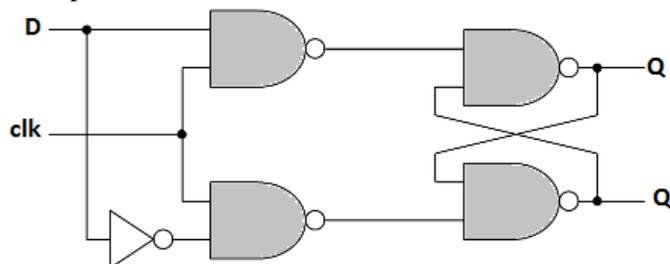
Figure 1. D-Latch Using NAND gates

A D-Flip-flop a positiveedge- triggered where two D latches are connected in series and a clock signal Clk is connected to the E input of the latches, one directly, and one through an inverter. The first latch is called the master latch. The master latch is enabled when Clk is 0 and follows the primary input D. When Clk is a 1, the master latch is disabled but the second latch, called the slave latch, is enabled so that the output from the master latch is transferred to the slave latch. The slave latch is enabled all the while that Clk is high, but its content changes only at the beginning of the cycle, that is, only at the rising edge of the signal because once Clk is high, the master latch is disabled and so the input to the slave latch will not change. The circuit of Figure 2 is called a positive edge-triggered flip-flop because the output Q on the slave latch changes only at the rising edge of the clock. If the slave latch is enabled when the clock is low, then it is referred to as a negative edge-triggered flip-flop. The circuit of Figure 2 is also referred to as a masterslave D flip-flop because of the two latches used in the circuit.
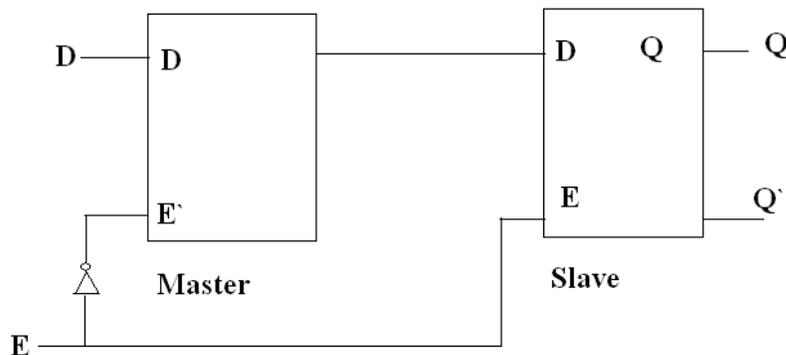
Figure 2 Master-slave positive-edge-triggered D flip-flop circuit using D latches;

A Bi-stable element, a simple sequential circuit or storage element which is constructed with two inverters connected sequentially in a loop as shown in figure 3.
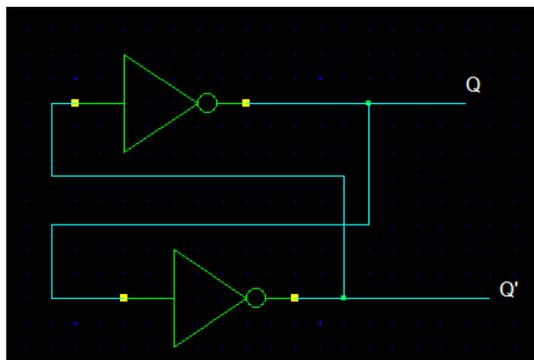
Figure 3. Two inverters back to back (Bistable element)

It has no inputs and two outputs labeled Q and Q'. Since the circuit has no inputs, we cannot change the values of Q and Q'. However, Q will take on whatever value it happens to be when the circuit is first powered up. Assume that Q = 0 when we switch on the power. Since Q is also the input to the bottom inverter, Q', therefore, is a 1. A 1 going to the input of the top inverter will produce a 0 at the output Q, which is what we started off with. Similarly, if we start the circuit with Q = 1, we will get Q' = 0, and again we get a stable situation. A bi-stable element has memory in the sense that it can remember the content (or state) of the circuit indefinitely. Using the signal Q as the state variable to describe the state of the circuit, we can say that the circuit has two stable states: Q = 0, and Q = 1; hence the name bi-stable. An analog analysis of a bi-stable element, however, reveals that it has three equilibrium points and not two as found from the digital analysis. Assuming again that Q = 1, and we plot the output voltage (Vout1) versus the input voltage (Vin1) of the top inverter, we get the solid line as shown in Figure 4. The dotted line shows the operation of the bottom inverter where Vout2 and Vin2 are the output and input voltages respectively for that inverter. Figure 4 shows that there are three intersection points, two of which corresponds to the two stable states of the circuit where Q is either 0 or 1. The third intersection point labeled meta-stable, is at a voltage that is neither a logical 1 nor a logical 0 voltage. Nevertheless, if we can get the circuit to operate at this voltage, then it can stay at that point indefinitely. Practically, however, we can never operate a circuit at precisely a certain voltage. A slight deviation from the meta-stable point as cause by noise in the circuit or other stimulants will cause the circuit to go to one of the two stable points. Once at the stable point, a slight deviation, however, will not cause the circuit to go away from the stable point but rather back towards the stable point because of the feedback effect of the circuit. In order for the element to change state, we need to apply a strong enough pulse satisfying a given minimum

width requirement. Otherwise, the element will either remain at the current state or go into the meta-stable state in which case unpredictable results can occur.
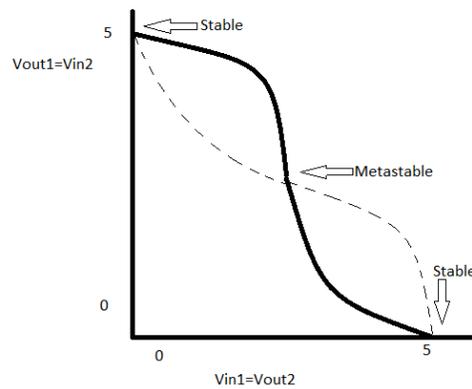
Figure 4**.** Analysis of bistable element
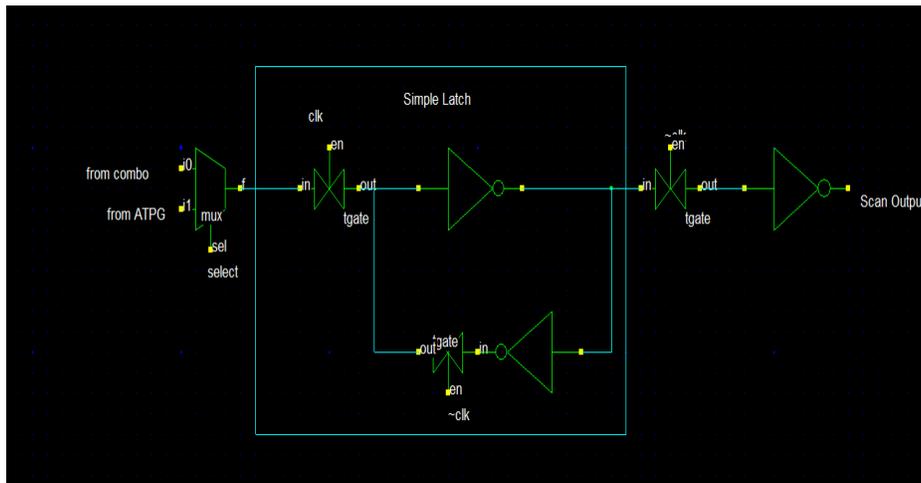
Figure 5. Proposed latch using lesser number of gates

 The proposed latch is as shown in figure 5 and the working is as follows: when your select pin is low the data in the logic is sent and the TG1 is on when the clock signal is low it passes and the bi-stable inverter and acts as a storage and passes it to the next clock cycle, where as when your clock goes low the clock signal is high, then the TG1 is open and TG2 is shorted and it retains its previous value. This is again passed to the next latch. If your scan enable is high the output from the combinational circuit is got and the scan out is passed to the combinational circuit and also the circuit is tested.

The major advantage of using a latch is it uses minimum number of gates, so they consume less chip area. The latches vary with variation with their outputs are constantly varying with respect to the input as long as the enable signal is high. Since they are smaller in size they consume less power. There are lesser number of gates there is less gate delay. They are level sensitive. Another major advantage is when the technology is very low, as the frequency is increasing, the supply voltage is less, then gate delay is increased.

3. 1.Software Used

T-Simulation Program with Integrated Circuit Emphasis (T-SPICE), which is used for the experimental results with maintaining accuracy for the results.

3.1.1 T-SPICE

Tanner tools comprise of L-edit, S-edit and LVS . S-Edit is for schematic capture. T-spice for Simulation, L-Edit for physical layout,W-Edit for waveform analysis, Hiper verify, L-Edit Standard DRC,L-Edit LVS for verification. T-Spice provides highly optimized code for evaluating device models, formulating the system of linear equations, and solving that system. T-spice uses advanced mathematical methods to achieve superior numerical stability. Hence large circuits and feedback circuit can be analyzed. T-spice uses very accurate numerical methods and change conservation to achieve superior simulation accuracy. T-Spice maintains compatibility with traditional circuit simulation tools, while using the best   available simulation technology to deliver results as quickly and accurately as possible. It handles most complex full custom IC schematic captures and also helps speed up design through tight iteration with simulation. It offers easy interoperability with third party tools and legacy data. It Simplifies schematics capture through a powerful ,easy to use interface and delivers an ideal performance to cost ratio easy to mange.

4. Experimental Results

When considering the proposed latch with T-Spice and with 250µm technology and 100MHz and 500MHz the result after the simulation is as shown in the figure with the supply voltage at 1.2v for an input bit as 0111101. The output at the W-Edit is shown for 100MHz in Figure 6 and the same for 500MHz in figure 7.The proposed latch reduces the number of gates when compared to a normal flip-flop and also the area is reduced. In a normal chip there will be lots of flip-flops that will be added during the scan and this reduces the overall area and the power dissipation. The set up time of a normal D-flip-flop is 65ps whereas for a latch it is 25ps and the clock to q delay are almost the same in both and D-to-Q delay for latches is 40ps.
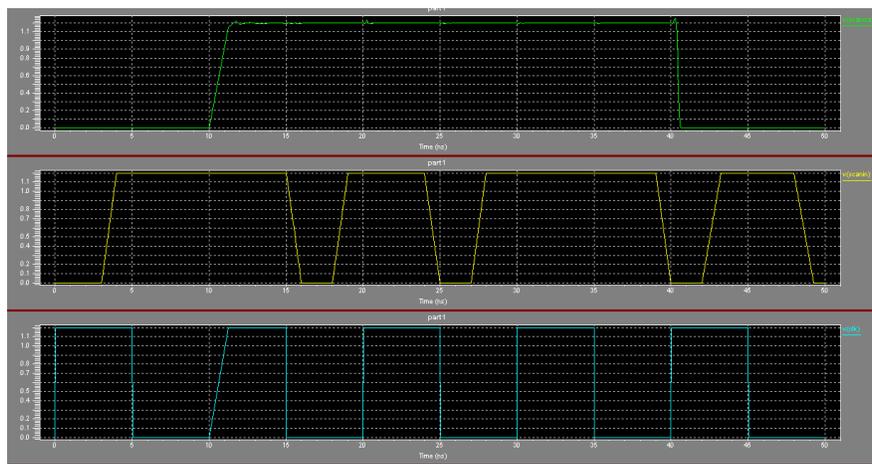
Figure 6. Post Simulation Result of Latch At 100mhz Using T-Spice
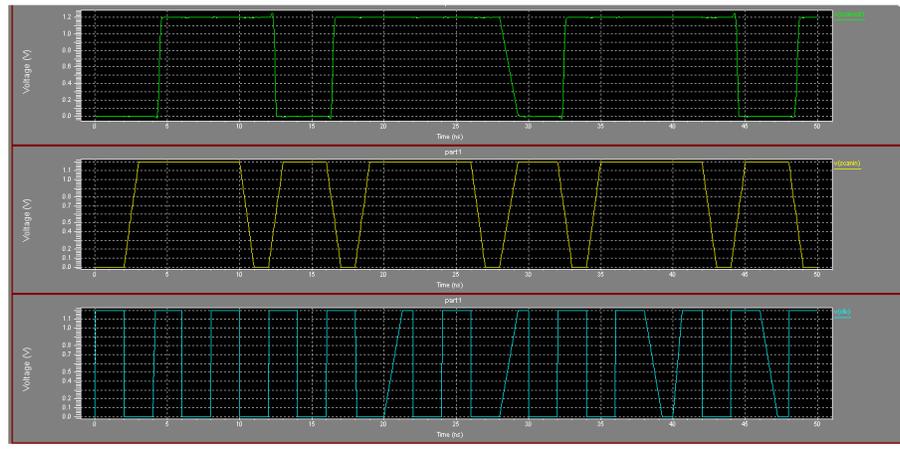
Figure 7. Post Simulation Result Of Latch At 500mhz Using T-Spice

5. CONCLUSIONS

The proposed latch consumes only 6 gates where as a normal d flip flop consists of 10 gates and the most commonly used D-Latch also uses 5 gates which not only increases the area as well as the gate delay but also the power consumed by these gates. The set up time of this latch is way less than the D flip flop and this increases the performance of the proposed latchas well. The latch has an issue that it changes with respect to the change with its input and not with respect to clock, but this is solved by placing the transmission gate at the input. This has an issue with the static timing analysis but still the overall area is reduced and the power consumption is reduced during the test mode.

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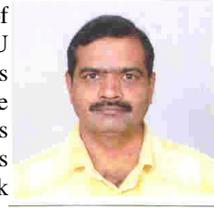
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